SAMSUNG

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MZ1L2960HCJR-00A07
MZ1L21T9HCLS-00A07
MZ1L23T8HBLA-00A07

# M.2 NVMe SSD Specification (PM9A3)

# Datasheet

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# Revision History

| Revision No. | History | Draft Date | Editor by | Review by |
|---|---|---|---|---|
| 1.0 | 1. Initial release. | Jan.22, 2021 | Semi Lee | Benjamin Lim |

| Part Number | Capacity | LBA (512B Bytes size) |
|---|---|---|
| MZ1L2960HCJR-00A07 | 960GB | 1,875,385,008 |
| MZ1L21T9HCLS-00A07 | 1920GB | 3,750,748,848 |
| MZ1L23T8HBLA-00A07 | 3840GB | 7,501,476,528 |

## FEATURES

· PCI Express Gen4
  - Single port x4 lanes
. Compliant with PCI Express Base Specification Rev. 4.0
· Compliant with NVM Express Specification Rev. 1.4
· Enhanced Power-Loss Data Protection
· End-to-End Data Protection
· Support SSD Enhanced S.M.A.R.T. Feature Set
· Hardware based AES-XTS 256-bit Encryption Engine
· Static and Dynamic Wear Leveling
· RoHS / Halogen-Free Compliant
· TCG Opal 2.0 Compliant

## DRIVE CONFIGURATION

| | |
|---|---|
| · Form Factor | M.2 |
| · Interface | PCI Express Gen4 x4 |
| · Bytes per Sector | 512(default), 4096 Bytes |

## PERFORMANCE SPECIFICATIONS[2)]

**Gen3**

· Data Transfer Rate (128KB data size)

| | |
|---|---|
| - Sequential Read | Up to 3500 MB/s[3)] |
| - Sequential Write | Up to 2000 MB/s |

· Data I/O Speed (4KB data size, Sustained)

| | |
|---|---|
| - Random Read | Up to 800K IOPS |
| - Random Write | Up to 85K KIOPS |

**Gen4**

· Data Transfer Rate (128KB data size)

| | |
|---|---|
| - Sequential Read | Up to 5500 MB/s[3)] |
| - Sequential Write | Up to 2000 MB/s |

· Data I/O Speed (4KB data size, Sustained)

| | |
|---|---|
| - Random Read | Up to 800K IOPS |
| - Random Write | Up to 85K KIOPS |

· Latency (Sustained workload)

| | |
|---|---|
| - Random Read/ Write (typical)[4)] | 75/30 us |
| - Sequential Read/ Write (typical)[5)] | 20/20 us |
| - Drive Ready Time (typical) | 5s |

## RELIABILITY SPECIFICATIONS

| | |
|---|---|
| · Uncorrectable Bit Error Rate | 1 sector per $10^{17}$ bits read |
| · MTBF | 2,000,000 hours |
| · Component Design Life | 5 years |
| · Endurance | |
| - 3840/1920/960GB | 1DWPD |
| · TBW (@4KB Random Write) | |
| - 3840GB | 7008 TB |
| - 1920GB | 3504 TB |
| - 960GB | 1752TB |
| · Data Retention | 3 months |

## ENVIRONMENTAL SPECIFICATIONS

| | |
|---|---|
| · Temperature, Case (Tc[6)]) | |
| - Operating | 0 ~ 70 °C |
| - Non-operating | -40 ~ 85 °C |
| · Humidity (non-condensing) | 5 ~ 95% |
| · Linear Shock (0.5ms duration with 1/2 sine wave) | |
| - Non-operating | 1,500 G |
| · Vibration | |
| - Non-operating (10 ~ 2,000 Hz, Sinusoidal) | 20 G |

## POWER REQUIREMENTS

| | |
|---|---|
| · Supply Voltage / Tolerance | 3.3V±5 % |
| · Active[7)] (max. RMS) | 8.2W |
| · Idle (typ.) | 2.5W |

## PHYSICAL DIMENSION

| | |
|---|---|
| · Width | 22.00 ± 0.15 mm |
| · Length | 110.00 ± 0.15 mm |
| · Thickness | 3.80 ± 0.18 mmT |
| · Weight | Up to 20 g |

## OPERATING SYSTEMS

RHEL 7.6/8.2
CentOS 7.6/8.2
Ubuntu 18.10/20.04
Windows Server 2016/2019

***NOTE:*** *Specifications are subject to change without notice.*

1) 1MB = 1,000,000 Bytes, 1GB = 1,000,000,000 Bytes, unformatted Capacity. User accessible capacity may vary depending on operating environment and formatting.
2) Based on PCI Express Gen3 x4, Random performance measured using FIO 2.1.3 in CentOS6(Kernel 3.14) with 4KB (4,096 bytes) of data transfer size in queue depth 32 by 4 workers and Sequential performance with 128KB (131,072 bytes) of data transfer size in queue depth 32 by 1 worker. Actual performance may vary depending on use conditions and environment.
3) 1 MB/sec = 1,000,000 bytes/sec was used in sequential performance.
4) The random latency is measured by using FIO 2.1.3 in Linux RHEL 6.6(Kernel 3.14.29) and 4KB (4,096 bytes) transfer size with queue depth 1 by 1 worker.
5) The Sequential latency is measured by using FIO 2.1.3 in CentOS6(Kernel 3.14) and 4KB (4,096 bytes) transfer size with queue depth 1 by 1 worker.
6) Tc is defined as the Max surface temperature of NAND packages. Sufficient cooling airflow or effective heat-dissipation add-on(i.e. heat sink or heat spreader) are recommended to be operated properly on heavier workloads wthin device operating temperature.
7) Active power is measured using IOMeter2006 on Windows Server 2012.

## Table Of Contents

# 1.0 INTRODUCTION

## 1.1 General Description

This document describes the specifications of the Samsung SSD PM9A3, which is a native-PCIe SSD for enterprise application.

The Samsung SSD PM9A3 presents outstanding performance with instant responsiveness to the host system, by applying the Peripheral Component Interconnect Express (PCIe) 3.0 interface standard, as well as highly efficient Non-Volatile Memory Express (NVMe) Protocol.

The Samsung SSD PM9A3 delivers wide bandwidth of up to 3,500MB/s for sequential read speed and up to 2,100MB/s for sequential write speed under up to 8.2W power. With the help of Toggle 2.0 NAND Flash interface, the Samsung SSD PM9A3 delivers random performance of up to 800KIOPS for random 4KB read and up to 85KIOPS for random 4KB write in the sustained state.

By combining the enhanced reliability Samsung NAND Flash memory silicon with NAND Flash management technologies, the Samsung SSD PM9A3 delivers the extended endurance of up to 1.3 drive writes per day over 3 years, which is suitable for enterprise applications, in M.2 form factor line ups: 960GB and 1920GB

In addition, the Samsung SSD PM9A3 supports Power Loss Protection (PLP). PLP solution can guarantee that data issued by the host system are written to the storage media without any loss in the event of sudden power off or sudden power failure.

## 1.2 Product List

[Table 1] Product List

| Type | Capacity | Part Number |
|---|---|---|
| M.2[1)] | 960GB | MZ1L2960HCJR-00A07 |
| | 1920GB | MZ1L21T9HCLS-00A07 |
| | 3840GB | MZ1L23T8HBLA-00A07 |

**NOTE:**
1) 22.00 ± 0.15 x 110.00 ± 0.15 x 3.80 ± 0.18

## 1.3 Ordering Information

| M | Z | X | X | X | X | X | X | X | X | X | X | - | X | X | X | X | X |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |

**1. Memory (M)**

**2. Module Classification**
Z: SSD

**3. Form Factor**
1: PCIe M.2 (22*110)

**4. Line-Up**
L: SV (VNAND 3bit MLC)

**5. SSD CTRL**
2: Elpis, S.LSI

**6~8. SSD Density**
960: 960GB
1T9: 1920GB
**3T8: 3840GB**

**9. NAND PKG + NAND Voltage**
H: BGA (LF,HF)

**10. Flash Generation**
C : 4th Generation

**11~12. NAND Density**
JR : 2T ODP 2CE (FBI)
LS : 4T HDP 2CE(FBI)
LA : 8T HDP 2CE(FBI)

**13. "-"**

**14. Default**
"0"

**15. HW revision**
0: No revision

**16. Packaging type**
A: Retail Packaging

**17~18. Customer**
07: General

# 2.0 PRODUCT SPECIFICATIONS

## 2.1 Capacity

[Table 2] User Capacity and Addressable Sectors

| Capacity[2)] | Max LBA[3)] |
|---|---|
| 960GB | 1,875,385,008 |
| 1920GB | 3,750,748,848 |
| 3840GB | 7,501,476,528 |

**NOTE:**
1) Gigabyte (GB) = 1,000,000,000 Bytes, 1 Sector = 512Bytes
2) Capacity shown in Table 2 represents the total usable capacity of the SSD which may be less than the total physical capacity. A certain area in physical capacity, not in the area shown to the user, might be used for the purpose of NAND flash management.
3) Max. LBA shown in Table 2 represents the total user addressable sectors in LBA mode and calculated by IDEMA rule.

## 2.2 Performance

[Table 3] Sustained Random Read/Write Performance (IOPS)

| Maximum Performance[1)] | Unit | Gen3 | | | Gen4 | | |
|---|---|---|---|---|---|---|---|
| | | 960GB | 1920GB | 3840GB | 960GB | 1920GB | 3840GB |
| Random 4KB Read (Up to) | IOPS | 550K | 800K | 800K | 550K | 800K | 800K |
| Random 4KB Write (Up to) | IOPS | 60K | 85K | 85K | 60K | 85K | 85K |

**NOTE:**
1) Random performance in Table 3 was measured by using FIO 2.7 in Linux Gen3: CentOS6(kernel 3.14) with 4KB (4,096 bytes) of data transfer size in Queue Depth=32 by 4 workers. Measurements were performed on a full Logical Block Address (LBA) span of the drive in sustained state. The actual performance may vary depending on use conditions and environment.

[Table 4] Sequential Read/Write Performance

| Maximum Performance[1)] | Unit | Gen3 | | | Gen4 | | |
|---|---|---|---|---|---|---|---|
| | | 960GB | 1920GB | 3840GB | 960GB | 1920GB | 3840GB |
| Sequential 128KB Read (Up to) | MB/s | 3500 | 3500 | 3500 | 5000 | 5500 | 5500 |
| Sequential 128KB Write (Up to) | MB/s | 1400 | 2000 | 2000 | 1400 | 2000 | 2000 |

**NOTE:**
1) Sequential performance inTable 4 was measured by using FIO 2.7 in Linux Gen3: CentOS6(kernel 3.14) with 128KB (131,072 bytes) of data transfer size in Queue Depth=32 by 1 worker.

[Table 5] IOPS Consistency

| Maximum Performance[1)] | 960GB | 1920GB | 3840GB |
|---|---|---|---|
| Random Read (4 KB) | 95% | 95% | 95% |
| Random Write (4 KB) | 95% | 95% | 95% |

**NOTE:**
1) IOPS consistency measured using FIO with queue depth 32.
2) IOPS Consistency (%) = (99.9% IOPS) / (Average IOPS) x 100.

## 2.3 Latency

[Table 6] Latency[1] (sustained state)

| Queue Depth = 1 | Unit | 960GB | 1920GB | 3840GB |
|---|---|---|---|---|
| Random Read/Write[2] | us | 75/30 | 75/30 | 75/30 |
| Sequential Read/Write[3] | us | 20/20 | 20/20 | 20/20 |
| Drive Ready Time[4] | sec | 5 | 5 | 5 |

**NOTE:**
1) Typical values.
2) The random latency is measured by using FIO 2.7 in Linux Gen3: CentOS6(kernel 3.14) and 4KB transfer size with queue depth 1 by 1 worker.
3) The sequential latency is measured by using FIO 2.7 in Linux Gen3: CentOS6(kernel 3.14) and 4KB transfer size with queue depth 1 by 1 worker.
4) The maximum taking time to be ready for receiving commands after power-up (CSTS.Ready=1). It is expected that I/O commands may not be completed at this point.

## 2.4 Quality of Service (QoS)

[Table 7] Quality of Service (QoS)

| Quality of Service (99%) | Unit | 960GB | 1920GB | 3840GB |
|---|---|---|---|---|
| Read(4KB, QD=1) | ms | 0.1 | 0.1 | 0.1 |
| Read(4KB, QD=32) | ms | 0.5 | 0.25 | 0.25 |
| Write(4KB, QD=1) | ms | 0.06 | 0.03 | 0.03 |
| Write(4KB, QD=32) | ms | 0.8 | 0.7 | 0.7 |

| Quality of Service (99.99%) | Unit | 960GB | 1920GB | 3840GB |
|---|---|---|---|---|
| Read(4KB, QD=1) | ms | 0.15 | 0.15 | 0.15 |
| Read(4KB, QD=32) | ms | 0.6 | 0.5 | 0.5 |
| Write(4KB, QD=1) | ms | 0.06 | 0.04 | 0.04 |
| Write(4KB, QD=32) | ms | 0.8 | 0.7 | 0.7 |

**NOTE:**
1) QoS is measured using FIO 2.7 in CentOS6 (Linux kernel 3.14) with queue depth 1, 32 on 4KB random read and write.
2) QoS is measured as the maximum round-trip time taken for 99 and 99.99% of commands to host.

# 2.5 Power

The Samsung SSD PM9A3 is implemented in standardized M.2 form factor and gets primary 3.3V power from the host system.
For 3.3V, the allowable voltage tolerance and noise level in SSD are described in chapter 2.5.1, the power consumption in 2.5.2 and the inrush current in 2.5.3.

## 2.5.1 Maximum Voltage Ratings (3.3V)

[Table 8] Allowable Voltage Tolerance[1)]

| Operating Voltage | 960GB | 1920GB | 3840GB |
|---|---|---|---|
| 3.3V | 5% | | |
| 3.3V Noise level | DC to 100Khz : 300 mVp-p Max<br>100Khz to 20Mhz : 50 mVp-p Max | | |
| 3.3V Min Off time | 10ms | | |

**NOTE:**
1) The components inside SSD were designed to endure the range of voltage fluctuations, which might be induced by the host system, in Table 6.

## 2.5.2 Power Consumption (3.3V)

In enterprise server and storage system, the Samsung SSD PM9A3 is designed for the specific usage, which means that SSD will be always operated by the host system during the entire life. Hence, the Samsung SSD PM9A3 does not manage any low power modes except for the Active/Idle and Off mode.

[Table 9] Power Consumption (3.3V Supply Voltage)[1)]

| Power Mode | | 960GB | 1920GB | 3840GB |
|---|---|---|---|---|
| Active[2)] | Read | 7.5W | 8.0W | 8.2W |
| | Write | 6.5W | 8.2W | 8.2W |
| Idle[3)] | | 2.5W | 2.5W | 2.5W |

**NOTE:**
1) Power consumption was measured in the 3.3V power pins of the connector plug in SSD. The active and idle power is defined as the highest averaged power value, which is the maximum RMS average value over 100 ms duration.
2) The measurement condition for active power is assumed for Maximum power between sequential or random performancein PCIe Gen4.
3) The idle state is defined as the state that the host system can issue any commands into SSD at any time.

## 2.5.3 Inrush Current

[Table 10] Inrush Current

| Inrush Current | 960GB | 1920GB | 3840GB |
|---|---|---|---|
| 3.3V | 1A | | |

## 2.5.4 Power Loss Protection

By using internal back-up power technology, the Samsung SSD PM9A3 supports power loss protection (PLP) feature to guarantee the reliability of data requested by the host system. When power is unpredictably lost, SSD can detect automatically this abnormal situation and transfer all user data and meta-data cached in DRAM into the Flash media during any SSD operations.

# 2.6 Reliability

The reliability specification of the Samsung SSD PM9A3 follows JEDEC standard, which are included in JESD218A and JESD219A documents

## 2.6.1 Mean Time Between Failures

By definition, Mean Time between Failures (MTBF) is the estimated time between failures occurring during SSD operation.

[Table 11] MTBF Specifications

| Parameter | 960GB | 1920GB | 3840GB |
|---|---|---|---|
| MTBF | 2,000,000 Hours | | |

## 2.6.2 Uncorrectable Bit Error Rate

By definition, Uncorrectable Bit Error Rate (UBER) is a metric for the rate of occurrence of data errors, equal to the number of data errors per bits read as specified in the JESD218 document of JEDEC standard.

[Table 12] UBER Specifications

| Parameter | 960GB | 1920GB | 3840GB |
|---|---|---|---|
| UBER | 1 sector per $10^{17}$ bits read | | |

## 2.6.3 Data Retention

By definition, data retention is the expected time period for retaining data in the SSD at the maximum rated endurance in power-off state as specified in the JESD218 document of JEDEC standard.

[Table 13] Data Retention

| Parameter | 960GB | 1920GB | 3840GB |
|---|---|---|---|
| Data Retention[1)] | 3 months | | |

**NOTE:**
1) Data retention was measured by assuming that SSD reaches the maximum rated endurance at 40C in power-off state.

## 2.6.4 Endurance

By definition, the endurance of SSD in enterprise application is defined as the maximum number of drive writes per day that can meet the requirements specified in the JESD218 document of JEDEC standard.

[Table 14] Drive Write Per Day (DWPD)

| Parameter | 960GB | 1920GB | 3840GB |
|---|---|---|---|
| DWPD | 1 drive writes per day over 5years | | |

[Table 15] TBW (Tera Bytes Written) Specifications

| Parameter | Unit | 960GB | 1920GB | 3840GB |
|---|---|---|---|---|
| TBW | TB | 1752 | 3504 | 7008 |

# 2.7 Environmental Specification

## 2.7.1 Temperature

[Table 16] Temperature, Case (Tc[1])

| Parameter | | 960GB | 1920GB | 3840GB |
|---|---|---|---|---|
| Temperature[1] | Operating | 0 to 70°C | | |
| | Non-operating | -40 to 85°C | | |

**NOTE:**
1) Tc is defined as the Max surface of NAND packages. Sufficient airflow is recommended to be operated properly on heavier workload within device operating temperature.

## 2.7.2 Dynamic Thermal Throttling

The dynamic thermal throttling (DTT) is implemented to prevent overheating. Table 17 shows the engaging and recovery temperature thresholds.

### 2.7.2.1 DTT table

[Table 17] Dynamic Thermal Throttling

| Step | Engaging temperature[1),2)] | Dis-engaging temperature | Performance[3)] |
|---|---|---|---|
| DTT1 | 77'C | 76'C | <85% |
| DTT2 | 81'C | 80'C | <50% |
| DTT3 | 83'C | 82'C | <25% |
| Critical (DTT4) | 85'C | 84'C | <1% |
| Shut-down[4)] | 93'C | N/A | N/A |
| Warning Composite Temperature (WCTEMP) | 77'C | | |
| Critical Composite Temperature (CCTEMP) | 85'C | | |

**NOTE:**
1) All temperatures are based on $T_{composite}$ values.
2) Recovering to the previous step as the temperature falls.
3) Throttling levels could be varying with workloads
4) Hanged/Halted. Recovering after power cycle.

### 2.7.2.2 Tcomposite

The Tcomposite is defined by the correlation equations as the below.
$T_{composite}$ = TS
where, TS means the temperature of reading in the thermal sensor on SSD.

## 2.7.3 Humidity

[Table 18] Humidity

| Parameter | | 960GB | 1920GB | 3840GB |
|---|---|---|---|---|
| Humidity[1] | Non-operating | 5% to 95% | | |

**NOTE:**
1) Humidity is measured in non-condensing state.

## 2.7.4 Shock and Vibration

[Table 19] Shock and Vibration

| Parameter | | 960GB | 1920GB | 3840GB |
|---|---|---|---|---|
| Shock[1] | Non-operating | 1,500 G | | |
| Vibration[2] | Non-operating | 20 G | | |

**NOTE:**
1) Test condition for shock: 0.5ms duration with half sine wave.
2) Test condition for vibration: 10Hz to 2000Hz.

# 3.0 MECHANICAL SPECIFICATIONS

## 3.1 Physical Information

The physical case of the Samsung SSD PM9A3 in M.2 form factor follows the standardized dimensions defined by SSD Form Factor Work Group

[Table 20] Physical Dimensions and Weightnical Outline

| Parameter | Unit | 960GB | 1920GB | 3840GB |
|---|---|---|---|---|
| Width | mm | 22.00 ± 0.15 | | |
| Length | mm | 110.00 ± 0.15 | | |
| Thickness | mm | 3.80 ± 0.18 | | |
| Weight | g | Up to 20.0g | | |

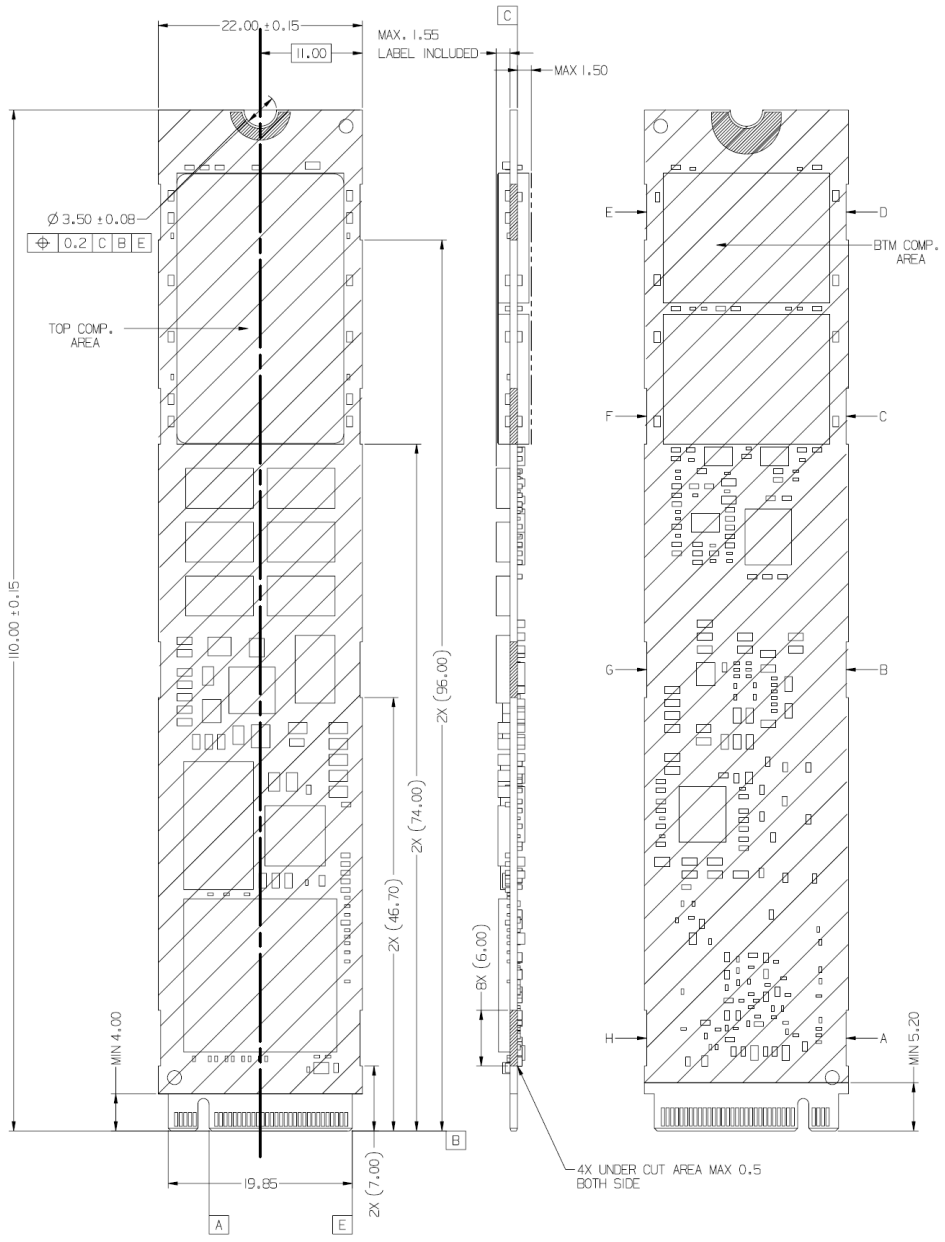



**Figure 1. Mechanical Outline 1**

# 4.0 INTERFACE SPECIFICATION

## 4.1 Connector Dimensions

Drive Connector: FOXCONN

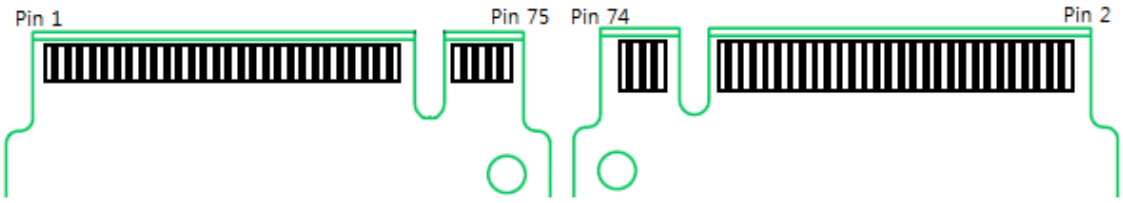



**Figure 2. M.2 Signal and Power pins**

## 4.2 Connector Pin Assignments

[Table 21] Certifications and Declarations

| Pin # | Assignment | Description | Pin # | Assignment | Description |
|---|---|---|---|---|---|
| 74 | 3.3 V | Primary Power | 75 | GND | Ground |
| 72 | 3.3 V | Primary Power | 73 | GND | Ground |
| 70 | 3.3 V | Primary Power | 71 | GND | Ground |
| 68 | SUSCLK | Floated | 69 | PEDET(NC-PCIe) | Floated |
| 58 | Reserved for MFG CLOCK | Floated | 67 | Not Used | |
| 56 | Reserved for MFG DATA | Floated | 57 | GND | Ground |
| 54 | PEWAKE# | Floated | 55 | REFCLKp | PCIe Reference Clock + |
| 52 | CLKREQ# | | 53 | REFCLKn | PCIe Reference Clock - |
| 50 | PERST# | | 51 | GND | Ground |
| 48 | Not Used | Floated | 49 | PERp0 | PCIe Receive- (lane 0) |
| 46 | Not Used | | 47 | PERn0 | PCIe Receive+ (lane 0) |
| 44 | ALERT# | SMBUS_alert | 45 | GND | Ground |
| 42 | SMDAT | SMBUS_data | 43 | PETp0 | PCIe Transmit+ (lane 0) |
| 40 | SMCLK | SMBUS_clock | 41 | PETn0 | PCIe Transmit- (lane 0) |
| 38 | Not Used | | 39 | GND | Ground |
| 36 | Not Used | | 37 | PERp1 | PCIe Receive- (lane 1) |
| 34 | Not Used | | 35 | PERn1 | PCIe Receive+ (lane 1) |
| 32 | Not Used | | 33 | GND | Ground |
| 30 | Not Used | | 31 | PETp1 | PCIe Transmit+ (lane 1) |
| 28 | Not Used | | 29 | PETn1 | PCIe Transmit- (lane 1) |
| 26 | Not Used | | 27 | GND | Ground |
| 24 | Not Used | | 25 | PERp2 | PCIe Receive- (lane 2) |
| 22 | Not Used | | 23 | PERn2 | PCIe Receive+ (lane 2) |
| 20 | Not Used | | 21 | GND | Ground |
| 18 | 3.3 V | Primary Power | 19 | PETp2 | PCIe Transmit+ (lane 2) |
| 16 | 3.3 V | Primary Power | 17 | PETn2 | PCIe Transmit- (lane 2) |
| 14 | 3.3 V | Primary Power | 15 | GND | Ground |
| 12 | 3.3 V | Primary Power | 13 | PERp3 | PCIe Receive- (lane 3) |
| 10 | LED1# | Drive Active Signal | 11 | PERn3[1)] | PCIe Receive+ (lane 3) |
| 8 | Not Used | | 9 | GND | Ground |
| 6 | Not Used | | 7 | PETp3 | PCIe Transmit+ (lane 3) |
| 4 | 3.3 V | Primary Power | 5 | PETn3 | PCIe Transmit- (lane 3) |

| | | | | | |
|---|---|---|---|---|---|
| 2 | 3.3 V | Primary Power | 3 | GND | Ground |
| | | | 1 | GND | Ground |

**NOTE:**
1) LED doesn't blink in Idle state.
LED blinking rate is 50ms(40 to 60ms) in Outstanding IO state(Read, Write).
LED blinking rate is 100ms(80 to 120ms) in following state(Sanitize, SMART Self-Test off-line, SCT WriteSame).

# 5.0 PCI and NVM EXPRESS REGISTERS

## 5.1 PCI Express Registers

### 5.1.1 PCI Register Summary

[Table 22] PCI Register Summary

| Start Address | End Address | Name | Type |
|---|---|---|---|
| 00h | 3Fh | PCI Header | PCI Configuration Header Space |
| 40h | 47h | PCI Power Management Capability | PCI Capability |
| 50h | 67h | MSI Capability | PCI Capability |
| 70h | A3h | PCI Express Capability | PCI Capability |
| B0h | BBh | MSI-X Capability | PCI Capability |
| 100h | 12Bh | Advanced Error Reporting (AER) Capability | PCI Extended Capability |
| 168h | 16Fh | Alternative Routing-ID (ARI) Capability | PCI Extended Capability |
| 178h | 18Bh | Secondary PCI Express Capability | PCI Extended Capability |
| 198h | 1BBh | Physical Layer 16.0 GT/s Capability | PCI Extended Capability |
| 1BCh | 1D3h | Margining Extended Capability Header | PCI Extended Capability |
| 3A0h | 3ABh | Data Link Feature Extended Capability | PCI Extended Capability |

### 5.1.2 PCI Header Registers

[Table 23] PCI Header Register Summary

| Start Address | End Address | Symbol | Description |
|---|---|---|---|
| 00h | 03h | ID | Identifiers |
| 04h | 05h | CMD | Command Register |
| 06h | 07h | STS | Device Status |
| 08h | 08h | RID | Revision ID |
| 09h | 0Bh | CC | Class Codes |
| 0Ch | 0Ch | CLS | Cache Line Size |
| 0Dh | 0Dh | MLT | Master Latency Timer |
| 0Eh | 0Eh | HTYPE | Header Type |
| 0Fh | 0Fh | BIST | Built in Self Test |
| 10h | 13h | MLBAR (BAR0) | Memory Register Base Address (lower 32-bit) |
| 14h | 17h | MUBAR (BAR1) | Memory Register Base Address (upper 32-bit) |
| 18h | 1Bh | IDBAR (BAR2) | Index/Data Pair Register Base Address |
| 1Ch | 1Fh | BAR3 | Reserved |
| 20h | 23h | BAR4 | Reserved |
| 24h | 27h | BAR5 | Reserved |
| 28h | 2Bh | CCPTR | CardBus CIS Pointer |
| 2Ch | 2Fh | SS | Subsystem Identifiers |
| 30h | 33h | EROM | Expansion ROM Base Address |
| 34h | 34h | CAP | Capabilities Pointer |
| 35h | 3Bh | RO | Reserved |
| 3Ch | 3Dh | INTR | Interrupt Information |
| 3Eh | 3Eh | MGNT | Minimum Grant |
| 3Fh | 3Fh | MLAT | Maximum Latency |

[Table 24] Identifier Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:16 | RO | A80Ah | Device ID |
| 0:15 | RO | 144Dh | Vendor ID |

[Table 25] Command Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:11 | RsvdP | 0h | Reserved |
| 10 | RW | 0h | Interrupt Disable |
| 9 | RO | 0h | Fast Back-to-Back Enable (N/A) |
| 8 | RW | 0h | SERR# Enable |
| 7 | RO | 0h | IDSEL Stepping/Wait Cycle Control (N/A) |
| 6 | RW | 0h | Parity Error Response Enable |
| 5 | RO | 0h | VGA Palette Snooping Enable (N/A) |
| 4 | RO | 0h | Memory Write and Invalidate Enable (N/A) |
| 3 | RO | 0h | Special Cycle Enable (N/A) |
| 2 | RW | 0h | Bus Master Enable |
| 1 | RW | 0h | Memory Space Enable |
| 0 | RW | 0h | I/O Space Enable |

[Table 26] Status Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15 | RW1C | 0h | Detected Parity Error |
| 14 | RW1C | 0h | Signaled System Error |
| 13 | RW1C | 0h | Received Master Abort |
| 12 | RW1C | 0h | Received Target Abort |
| 11 | RO | 0h | Reserved |
| 10:9 | RO | 0h | DEVSEL Timing (N/A) |
| 8 | RW1C | 0h | Master Data Parity Error Detected |
| 7 | RO | 0h | Fast Back-to-Back Transaction Capable (N/A) |
| 6 | RsvdZ | 0h | Reserved |
| 5 | RO | 0h | 66MHz Capable (N/A) |
| 4 | RO | 1h | Capabilities List |
| 3 | RO | 0h | Interrupt Status |
| 2:1 | RsvdZ | 0h | Reserved |
| 0 | RO | 0h | Reserved |

[Table 27] Revision ID Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 7:0 | RO | 0h | Controller Hardware Revision ID |

[Table 28] Class Code Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 23:16 | RO | 1h | Base Class Code |
| 15:8 | RO | 8h | Sub Class Code |
| 7:0 | RO | 2h | Programming Interface |

[Table 29] Cache Line Size Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 7:0 | RW | 0h | Cache Line Size (N/A) |

[Table 30] Master Latency Timer Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 7:0 | RO | 0h | Master Latency Timer (N/A) |

[Table 31] Header Type Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 7 | RO | 0h | Multi-Function Device |
| 6:0 | RO | 0h | Header Layout |

[Table 32] Built In Self Test Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 7 | HwInit | 0h | Built In Self Test (N/A) |
| 6 | RW/RO | 0h | Start BIST (N/A) |
| 5:4 | RsvdP | 0h | Reserved |
| 3:0 | RO | 0h | Completion Code (N/A) |

[Table 33] Memory Register Base Address Lower 32-bits (BAR0) Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:14 | RW | 0h | Base Address |
| 13:4 | RO | 0h | Reserved |
| 3 | RO | 0h | Pre-Fetchable |
| 2:1 | RO | 2h | Address Type (64-bit) |
| 0 | RO | 0h | Memory Space Indicator (MEMSI) |

[Table 34] Memory Register Base Address Upper 32-bits (BAR1)

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:0 | RO | 0h | Base Address |

[Table 35] Index/Data Pair Register Base Address (BAR2) Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:0 | RO | 0h | N/A |

[Table 36] BAR3 Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:0 | RO | 0h | N/A |

[Table 37] Vendor Specific BAR4 Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:0 | RO | 0h | N/A |

[Table 38] Vendor Specific BAR5 Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:0 | RO | 0h | N/A |

[Table 39] Cardbus CIS Pointer Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:0 | RO | 0h | N/A |

[Table 40] Subsystem Identifier Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:16 | RO | A812h | Subsystem ID |
| 15:0 | RO | 144Dh | Subsystem Vendor ID |

[Table 41] Expansion ROM Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:17 | RW | 0h | Expansion ROM Base Address |
| 16:1 | RO | 0h | Reserved |
| 0 | RW | 0h | Expansion ROM Enable/Disable |

[Table 42] Capabilities Pointer Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 7:0 | RO | 40h | Capability Pointer<br>(Points to PCI Power Management Capability Offset) |

[Table 43] Interrupt Information Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:8 | RO | 01h | Interrupt Pin |
| 7:0 | RW | FFh | Interrupt Line |

[Table 44] Minimum Grant Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 7:0 | RO | 0h | Minimum Grant (N/A) |

[Table 45] Maximum Latency Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 7:0 | RO | 0h | Maximum Latency (N/A) |

## 5.1.3 PCI Power Management Registers

[Table 46] PCI Power Management Capability Register Summary

| Start Address | End Address | Symbol | Description |
|---|---|---|---|
| 40h | 40h | PCIPM_ID | PCI Power Management Capability ID |
| 41h | 41h | NEXTCAP | Next Capability Pointer |
| 42h | 43h | PCIPM_CAP | PC Power Management Capabilities |
| 44h | 45h | PCIPM_CS | PCI Power Management Control and Status |
| 46h | 46h | PCIPM_CSR_BSE | PMCSR_BSE Bridge Extensions |
| 47h | 47h | PCIEPM_DATA | Data |

[Table 47] PCI Power Management Capability ID Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:8 | RO | 50h | Next Capability |
| 7:0 | RO | 1h | Capability ID |

[Table 48] PCI Power Management Capability Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:11 | RO | 0h | PME Support |
| 10 | RO | 0h | D2 Support |
| 9 | RO | 0h | D1 Support |
| 8:6 | RO | 0h | AUX Current |
| 5 | RO | 0h | Device Specific Initialization |
| 4 | RO | 0h | Immediate Readiness on Return to D0 |
| 3 | RO | 0h | PME Clock (N/A) |
| 2:0 | RO | 3h | Version (Support for PCIe Power Management Interface Spec revision 1.2) |

[Table 49] PCI Power Management Control and Status Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:24 | RO | 0h | Data register (N/A) |
| 23 | RO | 0h | Bus Power/Clock Enable (N/A) |
| 22 | RO | 0h | B2 , B3 support (N/A) |
| 21:16 | RsvdP | 0h | Reserved |
| 15 | RW1CS | 0h | PME_Status |
| 14:13 | RO | 0h | Data Scale (N/A) |
| 12:9 | RO | 0h | Data Select (N/A) |
| 8 | RW1CS | 0h | PME enable |
| 7:4 | RsvdP | 0h | Reserved |
| 3 | RO | 1h | No Soft Reset |
| 2 | RsvdP | 0h | Reserved |
| 1:0 | RW | 0h | Power State |

## 5.1.4 Message Signaled Interrupt Registers

[Table 50] Message Signaled Interrupt Capability Register Summary

| Start Address | End Address | Symbol | Description |
|---|---|---|---|
| 50h | 51h | MSI_ID | Message Signaled Interrupt Capability ID |
| 52h | 53h | MSI_MC | Message Signaled Interrupt Message Control |
| 54h | 57h | MSI_MA | Message Signaled Interrupt Message Address |
| 58h | 5Bh | MSI_MUA | Message Signaled Interrupt Upper Address |
| 5Ch | 5Dh | MSI_MDATA | Message Signaled Interrupt Message Data |
| 60h | 63h | MSI_MMASK | Message Signaled Interrupt Mask Bits |
| 64h | 67h | MSI_MPEND | Message Signaled Interrupt Pending Bits |

[Table 51] Message Signaled Interrupt Capability ID Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:8 | RO | 70h | Next Capability |
| 7:0 | RO | 05h | Capability ID |

[Table 52] Message Signaled Interrupt Control Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:11 | RsvdP | 0h | Reserved |
| 10 | RW | 0h | Extended Message Data Enable |
| 9 | RO | 0h | Extended Message Data Capable |
| 8 | RO | 0h | Per Vector Masking Capable |
| 7 | RO | 1h | 64-bit Address Capable |
| 6:4 | RW | 0h | Multiple Message Enable |
| 3:1 | RO | 5h | Multiple Message Capable |
| 0 | RW | 0h | MSI Enable |

[Table 53] Message Signaled Interrupt Lower Address Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:2 | RW | 0h | Message Address |
| 1:0 | RsvdP | 0h | Reserved |

[Table 54] Message Signaled Interrupt Upper Address Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:0 | RW | 0h | Message Upper Address |

[Table 55] Message Signaled Interrupt Message Data Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:16 | RW | 0h | Extended Message Data |
| 0:15 | RW | 0h | Data |

[Table 56] Message Signaled Interrupt Mask Bits Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:0 | RW | 0h | Mask Bits |

[Table 57] Message Signaled Interrupt Pending Bits Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:0 | RO | 0h | Pending Bits |

## 5.1.5 PCI Express Capability Registers

[Table 58] PCI Express Capability Register Summary

| Start Address | End Address | Symbol | Description |
|---|---|---|---|
| 70h | 71h | PCIE_ID | PCI Express Capability ID |
| 72h | 73h | PCIE_CAP | PCI Express Capabilities |
| 74h | 77h | PCIE_DCAP | PCI Express Device Capabilities |
| 78h | 79h | PCIE_DC | PCI Express Device Control |
| 7Ah | 7Bh | PCIE_DS | PCI Express Device Status |
| 7Ch | 7Fh | PCIE_LCAP | PCI Express Link Capabilities |
| 80h | 81h | PCIE_LC | PCI Express Link Control |
| 82h | 83h | PCIE_LS | PCI Express Link Status |
| 94h | 97h | PCIE_DCAP2 | PCI Express Device Capabilities 2 |
| 98h | 99h | PCIE_DC2 | PCI Express Device Control 2 |
| 9Ah | 9Bh | PCIE_DS2 | PCI Express Device Status 2 |
| 9Ch | 9Fh | PCIE_LCAP2 | PCI Express Link Capabilities 2 |
| A0h | A1h | PCIE_LC2 | PCI Express Link Control 2 |
| A2h | A3h | PCIE_LS2 | PCI Express Link Status 2 |

[Table 59] PCI Express Capability ID Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:8 | RO | B0h | Next Pointer (MSI-X Capability) |
| 7:0 | RO | 10h | Capability ID |

[Table 60] PCI Express Capabilities Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15 | RsvdP | 0h | Reserved |
| 14 | RO | 0h | Reserved |
| 13:9 | RO | 0h | Interrupt Message Number |
| 8 | HwInit | 0h | Slot Implementation (N/A) |
| 7:4 | RO | 0h | Device/Port Type |
| 3:0 | RO | 2h | Capability Version |

[Table 61] PCI Express Device Capabilities Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:29 | RsvdP | 0h | Reserved |
| 28 | RO | 1h | Function Level Reset Capability |
| 27:26 | RO | 0h | Captured Slot Power Limit Scale |
| 25:18 | RO | 0h | Captured Slot Power Limit Value |
| 17:16 | RsvdP | 0h | Reserved |
| 15 | RO | 1h | Role-based Error Reporting |
| 14:12 | RO | 0h | Reserved |
| 11:9 | RO | 7h | Endpoint L1 Acceptable Latency |
| 8:6 | RO | 7h | Endpoint L0 Acceptable Latency |
| 5 | RO | 1h | Extended Tag Field Supported |
| 4:3 | RO | 0h | Phantom Functions Supported |
| 2:0 | RO | 1h | Max Payload Size Supported (256 byte payload) |

[Table 62] PCI Express Device Control Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15 | RO | 0h | Initiate Function Level Reset |
| 14:12 | RW | 2h | Max Read Request Size |
| 11 | RW | 1h | Enable No Snoop |
| 10 | RWS | 0h | Aux Power PM Enable (N/A) |
| 9 | RW | 0h | Phantom Functions Enable (N/A) |
| 8 | RW | 1h | Extended Tag Enable |
| 7:5 | RW | 0h | Max Payload Size |
| 4 | RW | 1h | Enable Relaxed Ordering |
| 3 | RW | 0h | Unsupported Request Reporting Enable |
| 2 | RW | 0h | Fatal Error Reporting Enable |
| 1 | RW | 0h | Non-Fatal Error Reporting Enable |
| 0 | RW | 0h | Correctable Error Reporting Enable |

[Table 63] PCI Express Device Status Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:7 | RsvdZ | 0h | Reserved |
| 6 | RO | 0h | Emergency Power Reduction Detected (N/A) |
| 5 | RO | 0h | Transactions Pending |
| 4 | RW | 0h | Aux Power Detected |
| 3 | RW1C | 0h | Unsupported Request Detected |
| 2 | RW1C | 0h | Fatal Error Detected |
| 1 | RW1C | 0h | Non-Fatal Error Detected |
| 0 | RW1C | 0h | Correctable Error Detected |

[Table 64] PCI Express Link Capabilities Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:24 | HwInit | 0h | Port Number(Port 0) |
| 23 | RsvdP | 0h | Reserved |
| 22 | HwInit | 1h | ASPM Optionality Compliance |
| 21 | RO | 0h | Link Bandwidth Notification Capability |
| 20 | RO | 0h | Data Link Layer Link Active Reporting Capable |
| 19 | RO | 0h | Surprise Down Error Reporting Capable |
| 18 | RO | 0h | Clock Power Management |
| 17:15 | RO | 6h | L1 Exit Latency |
| 14:12 | RO | 7h | L0s Exit Latency |
| 11:10 | RO | 0h | Active State Power Management Support |
| 9:4 | RO | 4h | Maximum Link Width - (x4 link) |
| 3:0 | RO | 4h | Supported Link Speeds - PCIe Gen3(3h), Gen4(4h) |

[Table 65] PCI Express Link Control Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:14 | RW/RsvdP | 0h | DRS Signaling Control (N/A) |
| 13:12 | RsvdP | 0h | Reserved |
| 11 | RsvdP | 0h | Link Autonomous Bandwidth Interrupt Enable (N/A) |
| 10 | RsvdP | 0h | Link Bandwidth Management Interrupt Enable (N/A) |
| 9 | RsvdP | 0h | Hardware Autonomous Width Disable |
| 8 | RW | 0h | Enable Clock Power Management |
| 7 | RW | 0h | Extended Sync |
| 6 | RW | 0h | Common Clock Configuration |
| 5 | RsvdP | 0h | Retrain Link (N/A) |
| 4 | RsvdP | 0h | Link Disable (N/A) |
| 3 | RW | 0h | Read Completion Boundary |
| 2 | RsvdP | 0h | Reserved |
| 1:0 | RW | 0h | Active State Power Management Control |

[Table 66] PCI Express Link Status Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15 | RO | 0h | Link Autonomous Bandwidth Status (N/A) |
| 14 | RO | 0h | Link Bandwidth Management Status (N/A) |
| 13 | RO | 0h | Data Link Layer Link Active |
| 12 | HwInit | 1h | Slot Clock Configuration |
| 11 | RO | 0h | Link Training (N/A) |
| 10 | RO | 0h | Reserved |
| 9:4 | RO | 1h | Negotiated Link Width |
| 3:0 | RO | 1h | Current Link Speed |

[Table 67] PCI Express Device Capabilities 2 Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31 | HwInit | 0h | FRS Supported |
| 30:27 | RsvdP | 0h | Reserved |
| 26 | RO | 0h | Emergency Power Reduction Initialization Required (N/A) |
| 25:24 | RO | 0h | Emergency Power Reduction Supported (N/A) |
| 23:22 | HwInit | 0h | Max End-End TLP Prefixes |
| 21 | HwInit | 0h | End-End TLP Prefix Supported |
| 20 | RO | 0h | Extended Format Field Supported |
| 19:18 | HwInit | 0h | OBFF Supported |
| 17 | HwInit | 0h | 10-Bit Tag Requester Supported |
| 16 | HwInit | 0h | 10-Bit Tag Completer Supported |
| 15:14 | HwInit | 0h | LN System CLS (N/A) |
| 13:12 | RO | 0h | TPH Completer Supported |
| 11 | RO | 1h | Latency Tolerance Reporting Supported |
| 10 | HwInit | 0h | No RO-enabled PR-PR Passing (N/A) |
| 9 | RO | 0h | 128-bit CAS Completer Supported |
| 8 | RO | 0h | 64-bit Atomic Op Completer Supported |
| 7 | RO | 0h | 32-bit Atomic Op Completer Supported |
| 6 | RO | 0h | Atomic Op Routing Supported (N/A) |
| 5 | RO | 0h | ARI Forwarding Supported (N/A) |
| 4 | RO | 1h | Completion Timeout Disable Supported |
| 3:0 | HwInit | Fh | Completion Timeout Ranges Supported |

PCI Express Device Control 2 Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15 | RsvdP | 0h | End-to-end TLP Prefix Blocking |
| 14:13 | RW/RsvdP | 0h | OBFF Enable |
| 12 | RW | 0h | 10-Bit Tag Requester Enable |
| 11 | RO | 0h | Emergency Power Reduction Request (N/A) |
| 10 | RW/RsvdP | 1h | Latency Tolerance Reporting Mechanism Enable |
| 9 | RW | 0h | IDO Completion Enable |
| 8 | RW | 0h | IDO Request Enable |
| 7 | RW | 0h | AtomicOp Egress Blocking (N/A) |
| 6 | RW | 0h | AtomicOp Requester Enable |
| 5 | RW | 0h | ARI Forwarding Enable (N/A) |
| 4 | RW | 0h | Completion Timeout Disable |
| 3:0 | RW | 0h | Completion Timeout Value |

[Table 68] PCI Express Device Status 2 Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:0 | RsvdZ | 0h | Reserved |

[Table 69] PCI Express Link Capabilities 2 Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31 | RO | 0h | DRS supported |
| 30:25 | RsvdP | 0h | Reserved |
| 24 | HWinit | 0h | Two Retimers Presence Detect Supported |
| 23 | HWinit | 0h | Retimer Presence Detect Supported |
| 22:16 | RO | 0h | Lower SKP OS Reception Supported Speed Vector |
| 15:9 | RO | 0h | Lower SKP OS Generation Supported Speed Vector |
| 8 | RO | 0h | Cross-Link Supported |
| 7:1 | RO | Fh | Supported Speeds Vector - PCIe Gen3(7h), Gen4(Fh) |
| 0 | RsvdP | 0 | Reserved |

[Table 70] PCI Express Link Control 2 Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:12 | RWS/RsvdP | 0h | Compliance De-emphasis |
| 11 | RWS/RsvdP | 0h | Compliance SOS |
| 10 | RWS/RsvdP | 0h | Enter Modified Compliance |
| 9:7 | RWS/RsvdP | 0h | Transmit Margin |
| 6 | HwInit | 0h | Selectable De-Emphasis (N/A) |
| 5 | RWS/RsvdP | 0h | Hardware Autonomous Speed Disable |
| 4 | RWS/RsvdP | 0h | Enter Compliance |
| 3:0 | RWS/RsvdP | 4h | Target Link Speed<br>1h: 2.5 GT/s (Gen 1)<br>2h: 5.0 GT/s (Gen 2)<br>3h: 8 GT/s (Gen 3)<br>4h: 16 GT/s (Gen 4) |

[Table 71] PCI Express Link Status 2 Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15 | RO | 0h | DRS Message Received (N/A) |
| 14:12 | RO | 0h | Downstream Componenet Present (N/A) |
| 11:10 | RsvdZ | 0h | Reserved |
| 9:8 | RO | 1h | Crosslink Resolution |
| 7 | ROS/RsvdZ | 0h | Two Retimers Presence Detected |
| 6 | ROS/RsvdZ | 0h | Retimer Presence Detected |
| 5 | RW1CS | 0h | Link Equalization Request |
| 4 | ROS | 0h | Equalization Phase 3 Successful |
| 3 | ROS | 0h | Equalization Phase 2 Successful |
| 2 | ROS | 0h | Equalization Phase 1 Successful |
| 1 | ROS | 0h | Equalization Complete |
| 0 | RO | 1h | Current De-Emphasis |

## 5.1.6 MSI-X Registers

[Table 72] MSI-X Capability Register Summary

| Start Address | End Address | Symbol | Description |
|---|---|---|---|
| B0h | B1h | MSIX_ID | MSI-X Capability ID |
| B2h | B3h | MSIX_CAP | MSI-X Message Control |
| B4h | B7h | MSIX_TBL | MSI-X Table Offset and Table BIR |
| B8h | BBh | MSIX_PBA | MSI-X PBA Offset and PBA BIR |

[Table 73] MSI-X Identifier Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:8 | RO | 00h | Next Capability |
| 7:0 | RO | 11h | Capability ID |

[Table 74] MSI-X Control Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15 | RW | 0h | MSI-X Enable |
| 14 | RW | 0h | Function Mask |
| 13:11 | RsvdP | 0h | Reserved |
| 10:0 | RO | 81h | Table Size |

[Table 75] MSI-X Table Offset Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:3 | RO | 600h | Table Offset |
| 2:0 | RO | 0h | Table BIR |

[Table 76] MSI-X Pending Bit Array Offset Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:3 | RO | 400h | Pending Bit Array Offset |
| 2:0 | RO | 0h | Pending Bit Array BIR |

## 5.1.7 Advanced Error Reporting Registers

[Table 77] Advanced Error Reporting Capability Register Summary

| Start Address | End Address | Symbol | Description |
|---|---|---|---|
| 100h | 103h | AER_ID | AER Capability ID |
| 104h | 107h | AER_UCES | AER Uncorrectable Error Status |
| 108h | 10Bh | AER_UCEM | AER Uncorrectable Error Mask |
| 10Ch | 10Fh | AER_UCESEV | AER Uncorrectable Error Severity |
| 110h | 113h | AER_CES | AER Correctable Error Status |
| 114h | 117h | AER_CEM | AER Correctable Error Mask |
| 118h | 11Bh | AER_CC | AER Advanced Error Capabilities and Control |
| 11Ch | 12Bh | AER_HL | AER Header Log |

[Table 78] AER Capability ID Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:20 | RO | 168h | Next Pointer<br>(Points to Alternative Routing-ID Capability Header Offset) |
| 19:16 | RO | 2h | Capability Version |
| 15:0 | RO | 1h | Capability ID |

[Table 79] AER Uncorrectable Error Status Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:27 | RsvdZ | 0h | Reserved |
| 26 | RW1CS | 0h | Poisoned TLP Egress Blocked Status |
| 25 | RW1CS | 0h | TLP Prefix Blocked Error Status |
| 24 | RW1CS | 0h | Atomic Op Egress Blocked Status |
| 23 | RW1CS | 0h | MC Blocked TLP Status |
| 22 | RW1CS | 0h | Uncorrectable Internal Error Status |
| 21 | RW1CS | 0h | ACS Violation Status |
| 20 | RW1CS | 0h | Unsupported Request Error Status |
| 19 | RW1CS | 0h | ECRC Error Status |
| 18 | RW1CS | 0h | Malformed TLP Status |
| 17 | RW1CS | 0h | Receiver Overflow Status |
| 16 | RW1CS | 0h | Unexpected Completion Status |
| 15 | RW1CS | 0h | Completer Abort Status |
| 14 | RW1CS | 0h | Completion Timeout Status |
| 13 | RW1CS | 0h | Flow Control Protocol Error Status |
| 12 | RW1CS | 0h | Poisoned TLP Status |
| 11:6 | RsvdZ | 0h | Reserved |
| 5 | RW1CS | 0h | Surprise Down Error Status (N/A) |
| 4 | RW1CS | 0h | Data Link Protocol Error Status |
| 3:1 | RsvdZ | 0h | Reserved |
| 0 | Undefined | 0h | Undefined |

[Table 80] AER Uncorrectable Error Mask Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:27 | RsvdZ | 0h | Reserved |
| 26 | RWS | 0h | Poisoned TLP Egress Blocked Mask |
| 25 | RWS | 0h | TLP Prefix Blocked Error Mask |
| 24 | RWS | 0h | Atomic Op Egress Blocked Mask |
| 23 | RWS | 0h | MC Blocked TLP Mask |
| 22 | RWS | 1h | Uncorrectable Internal Error Mask |
| 21 | RWS | 0h | ACS Violation Mask |
| 20 | RWS | 0h | Unsupported Request Error Mask |
| 19 | RWS | 0h | ECRC Error Mask |
| 18 | RWS | 0h | Malformed TLP Mask |
| 17 | RWS | 0h | Receiver Overflow Mask |
| 16 | RWS | 0h | Unexpected Completion Mask |
| 15 | RWS | 0h | Completer Abort Mask |
| 14 | RWS | 0h | Completion Timeout Mask |
| 13 | RWS | 0h | Flow Control Protocol Error Mask |
| 12 | RWS | 0h | Poisoned TLP Mask |
| 11:6 | RsvdZ | 0h | Reserved |
| 5 | RWS | 0h | Surprise Down Error Mask (N/A) |
| 4 | RWS | 0h | Data Link Protocol Error Mask |
| 3:1 | RsvdZ | 0h | Reserved |
| 0 | Undefined | 0h | Undefined |

[Table 81] AER Uncorrectable Error Severity Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:27 | RsvdP | 0h | Reserved |
| 26 | RWS | 0h | Poisoned TLP Egress Blocked Severity |
| 25 | RWS | 0h | TLP Prefix Blocked Error Severity |
| 24 | RWS | 0h | Atomic Op Egress Blocked Severity |
| 23 | RWS | 0h | MC Blocked TLP Severity |
| 22 | RWS | 1h | Uncorrectable Internal Error Severity |
| 21 | RWS | 0h | ACS Violation Severity |
| 20 | RWS | 0h | Unsupported Request Error Severity |
| 19 | RWS | 0h | ECRC Error Severity |
| 18 | RWS | 1h | Malformed TLP Severity |
| 17 | RWS | 1h | Receiver Overflow Severity |
| 16 | RWS | 0h | Unexpected Completion Severity |
| 15 | RWS | 0h | Completer Abort Severity |
| 14 | RWS | 0h | Completion Timeout Severity |
| 13 | RWS | 1h | Flow Control Protocol Error Severity |
| 12 | RWS | 0h | Poisoned TLP Severity |
| 11:6 | RsvdP | 0h | Reserved |
| 5 | RWS | 1h | Surprise Down Error Severity (N/A) |
| 4 | RWS | 1h | Data Link Protocol Error Severity |
| 3:1 | RsvdP | 0h | Reserved |
| 0 | Undefined | 0h | Undefined |

[Table 82] AER Correctable Error Status Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:16 | RsvdZ | 0h | Reserved |
| 15 | RW1CS | 0h | Header Log Overflow Status |
| 14 | RW1CS | 0h | Corrected Internal Error Status |
| 13 | RW1CS | 0h | Advisory Non-Fatal Error Status |
| 12 | RW1CS | 0h | Replay Timer Timeout Status |
| 11:9 | RsvdZ | 0h | Reserved |
| 8 | RW1CS | 0h | Replay Number Rollover Status |
| 7 | RW1CS | 0h | Bad DLLP Status |
| 6 | RW1CS | 0h | Bad TLP Status |
| 5:1 | RsvdZ | 0h | Reserved |
| 0 | RW1CS | 0h | Received Error Status |

[Table 83] AER Correctable Error Mask Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:16 | RsvdP | 0h | Reserved |
| 15 | RWS | 1h | Header Log Overflow Status |
| 14 | RWS | 1h | Corrected Internal Error Mask |
| 13 | RWS | 1h | Advisory Non-Fatal Error Mask |
| 12 | RWS | 0h | Replay Timer Timeout Mask |
| 11:9 | RsvdP | 0h | Reserved |
| 8 | RWS | 0h | Replay Number Rollover Mask |
| 7 | RWS | 0h | Bad DLLP Mask |
| 6 | RWS | 0h | Bad TLP Mask |
| 5:1 | RsvdP | 0h | Reserved |
| 0 | RWS | 0h | Received Error Mask |

[Table 84] AER Capabilities and Control Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:13 | RsvdP | 0h | Reserved |
| 12 | RO | 0h | Completion Timeout Prefix/Header Log Capable |
| 11 | ROS | 0h | TLP Prefix Log Present |
| 10 | RWS | 0h | Multiple Header Recording Enable |
| 9 | RO | 1h | Multiple Header Recording Capable |
| 8 | RWS | 0h | ECRC Check Enable |
| 7 | RO | 1h | ECRC Check Capable |
| 6 | RWS | 0h | ECRC Generation Enable |
| 5 | RO | 1h | ECRC Generation Capable |
| 4:0 | ROS | 0h | First Error Pointer |

[Table 85] AER Header Log Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 127:120 | ROS | 0h | Header Byte 0 |
| 119:112 | ROS | 0h | Header Byte 1 |
| 111:104 | ROS | 0h | Header Byte 2 |
| 103:96 | ROS | 0h | Header Byte 3 |
| 95:88 | ROS | 0h | Header Byte 4 |
| 87:80 | ROS | 0h | Header Byte 5 |
| 79:72 | ROS | 0h | Header Byte 6 |
| 71:64 | ROS | 0h | Header Byte 7 |
| 63:56 | ROS | 0h | Header Byte 8 |
| 55:48 | ROS | 0h | Header Byte 9 |
| 47:40 | ROS | 0h | Header Byte 10 |
| 39:32 | ROS | 0h | Header Byte 11 |
| 31:24 | ROS | 0h | Header Byte 12 |
| 23:16 | ROS | 0h | Header Byte 13 |
| 15:8 | ROS | 0h | Header Byte 14 |
| 7:0 | ROS | 0h | Header Byte 15 |

## 5.1.8 Alternative Routing-ID (ARI) Capability Registers

[Table 86] Alternative Routing-ID (ARI) Capability Summary

| Start Address | End Address | Symbol | Description |
|---|---|---|---|
| 168h | 16Bh | ARI_ID | Alternative Routing-ID (ARI) Capability Header |
| 16Ch | 16Dh | ARI_CAP | ARI Capability Register |
| 16Eh | 16Fh | ARI_CON | ARI Control Register |

[Table 87] Alternative Routing-ID (ARI) Capability Header

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:20 | RO | 178h | Next Capability Offset<br>(Points to Secondary PCI Express Extended capability Header Offset) |
| 19:16 | RO | 1h | Capability Version |
| 15:0 | RO | Eh | PCI Express Extended Capability ID |

[Table 88] Alternative Routing-ID (ARI) Capability Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:8 | RO | 0h | Next Function Number |
| 7:2 | RsvdP | 0h | Reserved |
| 1 | RO | 0h | ACS Function Groups Capability (A) |
| 0 | RO | 0h | MFVC Function Groups Capability (M) |

[Table 89] Alternative Routing-ID (ARI) Control Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:7 | RsvdP | 0h | Reserved |
| 6:4 | RO | 0h | Function Group |
| 3:2 | RsvdP | 0h | Reserved |
| 1 | RO | 0h | ACS Function Groups Enable (A) |
| 0 | RO | 0h | MFVC Function Groups Enable (M) |

## 5.1.9 Secondary PCI Express Capability Registers

[Table 90] Secondary PCI Express Capability Register Summary

| Start Address | End Address | Symbol | Description |
|---|---|---|---|
| 178h | 17Bh | SPE_ID | Secondary PCI Express Capability |
| 17Ch | 17Fh | PCIE_LC3 | PCI Express Link Control 3 |
| 180h | 183h | PCIE_LE | PCI Express Lane Error Status |
| 184h | 185h | PCIE_L0EC | PCI Express Lane 0 Equalization Control |
| 186h | 187h | PCIE_L1EC | PCI Express Lane 1 Equalization Control |
| 188h | 189h | PCIE_L2EC | PCI Express Lane 2 Equalization Control |
| 18Ah | 18Bh | PCIE_L3EC | PCI Express Lane 3 Equalization Control |

[Table 91] Secondary PCI Express Capability ID Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:20 | RO | 198h | Next Pointer – Gen4(198h), Gen3(0h) |
| 19:16 | RO | 1h | Capability Version |
| 15:0 | RO | 19h | Capability ID (Secondary PCI Express Extended capability) |

[Table 92] PCI Express Link Control 3 Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:16 | Rsvdp | 0h | Reserved |
| 15:9 | RW | 0h | Enable Lower SKP OS Generation Vector |
| 8:2 | RsvdP | 0h | Reserved |
| 1 | RW | 0h | Link Equalization Request Interrupt Enable |
| 0 | RW | 0h | Perform Equalization (N/A) |

[Table 93] PCI Express Lane Error Status Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:4 | Rsvdp | 0h | Reserved |
| 3:0 | RW1CS | 0h | Lane Error Status Bits |

[Table 94] PCI Express Lane 0 Equalization Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15 | RsvdP | 0h | Reserved |
| 14:12 | HwInit/RO | 7h | Upstream Port 8.0T/s Receiver Preset Hint |
| 11:8 | HwInit/RO | 4h | Upstream Port 8.0T/s Transmitter Preset |
| 7 | RsvdP | 0h | Reserved |
| 6:4 | HwInit/RsvdP | 0h | Downstream Port 8.0T/s Receiver Preset Hint (N/A) |
| 3:0 | HwInit/RsvdP | 0h | Downstream Port 8.0T/s Transmitter Preset (N/A) |

[Table 95] PCI Express Lane 1 Equalization Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15 | RsvdP | 0h | Reserved |
| 14:12 | HwInit/RO | 7h | Upstream Port 8.0T/s Receiver Preset Hint |
| 11:8 | HwInit/RO | 4h | Upstream Port 8.0T/s Transmitter Preset |
| 7 | RsvdP | 0h | Reserved |
| 6:4 | HwInit/RsvdP | 0h | Downstream Port 8.0T/s Receiver Preset Hint (N/A) |
| 3:0 | HwInit/RsvdP | 0h | Downstream Port 8.0T/s Transmitter Preset (N/A) |

[Table 96] PCI Express Lane 2 Equalization Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15 | RsvdP | 0h | Reserved |
| 14:12 | HwInit/RO | 7h | Upstream Port 8.0T/s Receiver Preset Hint |
| 11:8 | HwInit/RO | 4h | Upstream Port 8.0T/s Transmitter Preset |
| 7 | RsvdP | 0h | Reserved |
| 6:4 | HwInit/RsvdP | 0h | Downstream Port 8.0T/s Receiver Preset Hint (N/A) |
| 3:0 | HwInit/RsvdP | 0h | Downstream Port 8.0T/s Transmitter Preset (N/A) |

[Table 97] PCI Express Lane 3 Equalization Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15 | RsvdP | 0h | Reserved |
| 14:12 | HwInit/RO | 7h | Upstream Port 8.0T/s Receiver Preset Hint |
| 11:8 | HwInit/RO | 4h | Upstream Port 8.0T/s Transmitter Preset |
| 7 | RsvdP | 0h | Reserved |
| 6:4 | HwInit/RsvdP | 0h | Downstream Port 8.0T/s Receiver Preset Hint (N/A) |
| 3:0 | HwInit/RsvdP | 0h | Downstream Port 8.0T/s Transmitter Preset (N/A) |

## 5.1.10 Physical Layer 16.0 GT/s Capability

[Table 98] Physical Layer 16.0 GT/s Capability Summary

| Start Address | End Address | Symbol | Description |
|---|---|---|---|
| 198h | 19Bh | | Physical Layer 16.0 GT/s Extended Capability Header |
| 19Ch | 19Fh | | 16.0 GT/s Capabilities Register |
| 1A0h | 1A3h | | 16.0 GT/s Control Register |
| 1A4h | 1A7h | | 16.0 GT/s Status Register |
| 1A8h | 1ABh | | 16.0 GT/s Local Data Parity Mismatch Status Register |
| 1ACh | 1AFh | | 16.0 GT/s First Retimer Data Parity Mismatch Status Register |
| 1B0h | 1B3h | | 16.0 GT/s Second Retimer Data Parity Mismatch Status Register |
| 1B4h | 1B7h | | Reserved |
| 1B8h | 1BBh | | 16.0 GT/s Control Register for Lane 0-3 |

[Table 99] Physical Layer 16.0 GT/s Extended Capability Header

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:20 | RO | 1BCh | Next Capability Offset |
| 19:16 | RO | 1h | Capability Version |
| 15:0 | RO | 26h | Capability ID (Secondary PCI Express Extended capability) |

[Table 100] 16.0 GT/s Capabilities Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:0 | RsvdP | 0 | Reserved |

[Table 101] 16.0 GT/s Control Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:0 | RsvdP | 0 | Reserved |

[Table 102] 16.0 GT/s Status Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:5 | RsvdZ | 0 | Reserved |
| 4 | RW1CS | 0 | Link Equalization Request 16.0 GT/s |
| 3 | ROS | 0 | Equalization 16.0 GT/s Phase 3 Successful |
| 2 | ROS | 0 | Equalization 16.0 GT/s Phase 2 Successful |
| 1 | ROS | 0 | Equalization 16.0 GT/s Phase 1 Successful |
| 0 | ROS | 0 | Equalization 16.0 GT/s Complete |

[Table 103] 16.0 GT/s Local Data Parity Mismatch Status Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:4 | RsvdP | 0 | Reserved |
| 3:0 | RW1CS | 0 | Local Data Parity Mismatch Status |

[Table 104] 16.0 GT/s First Retimer Data Parity Mismatch Status Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:4 | RsvdP | 0 | Reserved |
| 3:0 | RW1CS | 0 | First Retimer Data Parity Mismatch Status |

[Table 105] 16.0 GT/s Second Retimer Data Parity Mismatch Status Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:4 | RsvdP | 0 | Reserved |
| 3:0 | RW1CS | 0 | Second Retimer Data Parity Mismatch Status |

[Table 106] Reserved

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:0 | RsvdP | 0 | Reserved |

[Table 107] 16.0 GT/s Control Register for Lane 0-3

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:28 | HwInit/RO | 4h | Upstream Port 16.0 GT/s Transmitter Preset Lane 3 |
| 27:24 | HwInit/RsvdP | 0h | Downstream Port 16.0 GT/s Transmitter Preset Lane 3 (N/A) |
| 23:20 | HwInit/RO | 4h | Upstream Port 16.0 GT/s Transmitter Preset Lane 2 |
| 19:16 | HwInit/RsvdP | 0h | Downstream Port 16.0 GT/s Transmitter Preset Lane 2 (N/A) |
| 15:12 | HwInit/RO | 4h | Upstream Port 16.0 GT/s Transmitter Preset Lane 1 |
| 11:8 | HwInit/RsvdP | 0h | Downstream Port 16.0 GT/s Transmitter Preset Lane 1 (N/A) |
| 7:4 | HwInit/RO | 4h | Upstream Port 16.0 GT/s Transmitter Preset Lane 0 |
| 3:0 | HwInit/RsvdP | 0h | Downstream Port 16.0 GT/s Transmitter Preset Lane 0 (N/A) |

## 5.1.11 Margining Extended Capability Header

[Table 108] Margining Extended Capability Header Summary

| Start Address | End Address | Symbol | Description |
|---|---|---|---|
| 1BCh | 1BFh | | Margining Extended Capability Header |
| 1C0h | 1C1h | | Margining Port Capabilities Register |
| 1C2h | 1C3h | | Margining Port Status Register |
| 1C4h | 1C5h | | Margining Lane Control Register (Lane 0) |
| 1C6h | 1C7h | | Margining Lane Status Register (Lane 0) |
| 1C8h | 1C9h | | Margining Lane Control Register (Lane 1) |
| 1CAh | 1CBh | | Margining Lane Status Register (Lane 1) |
| 1CCh | 1CDh | | Margining Lane Control Register (Lane 2) |
| 1CEh | 1CFh | | Margining Lane Status Register (Lane 2) |
| 1D0h | 1D1h | | Margining Lane Control Register (Lane 3) |
| 1D2h | 1D3h | | Margining Lane Status Register (Lane 3) |

[Table 109] Physical Layer 16.0 GT/s Margining Capability

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:20 | RO | 3A0h | Next Capability Offset |
| 19:16 | RO | 1h | Capability Version |
| 15:0 | RO | 27h | PCI Express Extended Capability ID |

[Table 110] Margining Port Capabilities Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:1 | RsvdP | 0 | Reserved |
| 0 | HWInit | 0 | Margining uses Driver Software |

[Table 111] Margining Port Status Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:2 | RsvdP | 0 | Reserved |
| 1 | RO | 0 | Margining Software Ready |
| 0 | RO | 0 | Margining Ready |

[Table 112] Margining Lane Control Register Lane 0

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:8 | RW | 9Ch | Margin Payload |
| 7 | RsvdP | 0 | Reserved |
| 6 | RW | 0 | Usage Model |
| 5:3 | RW | 7h | Margin Type |
| 2:0 | RW | 0 | Receiver Number |

[Table 113] Margining Lane Status Register Lane 0

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:8 | RW | 0 | MarginPayload Status |
| 7 | RsvdP | 0 | Reserved |
| 6 | RW | 0 | Usage Model Status |
| 5:3 | RW | 0 | Margin Type Status |
| 2:0 | RW | 0 | Receiver Number Status |

[Table 114] Margining Lane Control Register Lane 1

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:8 | RW | 9Ch | Margin Payload |
| 7 | RsvdP | 0 | Reserved |
| 6 | RW | 0 | Usage Model |
| 5:3 | RW | 7h | Margin Type |
| 2:0 | RW | 0 | Receiver Number |

[Table 115] Margining Lane Status Register Lane 1

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:8 | RW | 0 | MarginPayload Status |
| 7 | RsvdP | 0 | Reserved |
| 6 | RW | 0 | Usage Model Status |
| 5:3 | RW | 0 | Margin Type Status |
| 2:0 | RW | 0 | Receiver Number Status |

[Table 116] Margining Lane Control Register Lane 2

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:8 | RW | 9Ch | Margin Payload |
| 7 | RsvdP | 0 | Reserved |
| 6 | RW | 0 | Usage Model |
| 5:3 | RW | 7h | Margin Type |
| 2:0 | RW | 0 | Receiver Number |

[Table 117] Margining Lane Status Register Lane 2

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:8 | RW | 0 | MarginPayload Status |
| 7 | RsvdP | 0 | Reserved |
| 6 | RW | 0 | Usage Model Status |
| 5:3 | RW | 0 | Margin Type Status |
| 2:0 | RW | 0 | Receiver Number Status |

[Table 118] Margining Lane Control Register Lane 3

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:8 | RW | 9Ch | Margin Payload |
| 7 | RsvdP | 0 | Reserved |
| 6 | RW | 0 | Usage Model |
| 5:3 | RW | 7h | Margin Type |
| 2:0 | RW | 0 | Receiver Number |

[Table 119] Margining Lane Status Register Lane 3

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 15:8 | RW | 0 | MarginPayload Status |
| 7 | RsvdP | 0 | Reserved |
| 6 | RW | 0 | Usage Model Status |
| 5:3 | RW | 0 | Margin Type Status |
| 2:0 | RW | 0 | Receiver Number Status |

## 5.1.12 Data Link Feature Extended Capability

[Table 120] ] Data Link Feature Extended Capability

| Start Address | End Address | Symbol | Description |
|---|---|---|---|
| 3A0h | 3A3h | | Data Link Feature Extended Capability Header |
| 3A4h | 3A7h | | Data Link Feature Capabilities Register |
| 3A8h | 3ABh | | Data Link Feature Status Register |

[Table 121] Data Link Feature Extended Capability Header

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31:20 | RO | 0h | Next Capability Offset |
| 19:16 | RO | 1h | Capability Version |
| 15:0 | RO | 25h | PCI Express Extended Capability ID |

[Table 122] Data Link Feature Capabilities Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31 | HwInit | 1h | Data Link Feature Exchange Enable |
| 30:23 | RsvdP | 0h | Reserved |
| 22:1 | RsvdP | 0h | Reserved |
| 0 | HwInit | 1h | Local Scaled Flow Control Supported |

[Table 123] Data Link Feature Status Register

| Bits | Type | Default Value | Description |
|---|---|---|---|
| 31 | RO | 0h | Remote Data Link Feature Supported Valid |
| 30:23 | RsvdP | 0h | Reserved |
| 22:1 | RO | 0h | Undefined |
| 0 | RO | 0h | Remote Scaled Flow Control Supported |

# 5.2 NVM Express Registers

## 5.2.1 Register Summary

[Table 124] Register Summary

| Start Address | End Address | Name | Type |
|---|---|---|---|
| 00h | 07h | CAP | Controller Capabilities |
| 08h | 0Bh | VS | Version |
| 0Ch | 0Fh | INTMS | Interrupt Mask Set |
| 10h | 13h | INTMC | Interrupt Mask Clear |
| 14h | 17h | CC | Controller Configuration |
| 18h | 1Bh | Reserved | Reserved |
| 1Ch | 1Fh | CSTS | Controller Status |
| 20h | 23h | NSSR | NVM Subsystem Reset |
| 24h | 27h | AQA | Admin Queue Attributes |
| 28h | 2Fh | ASQ | Admin Submission Queue Base Address |
| 30h | 37h | ACQ | Admin Completion Queue Base Address |
| 38h | EFFh | Reserved | Reserved |
| F00h | FFFh | Reserved | Command Set Specific |
| 1000h | 1003h | SQ0TDBL | Submission Queue 0 Tail Doorbell (Admin) |
| 1000h + (1 * (4 << CAP.DSTRD)) | 1003h + (1 * (4 << CAP.DSTRD)) | CQ0HDBL | Completion Queue 0 Head Doorbell (Admin) |
| ... | | | |
| 1000h+ (2y * (4 << CAP.DSTRD)) | 1003h + (2y * (4 << CAP.DSTRD)) | SQyTDVL | Submission Queue y Tail Doorbell |
| 1000h + ((2y + 1) * (4 << CAP.DSTRD)) | 1003h + ((2y + 1) * (4 << CAP.DSTRD)) | CQYHDBL | Completion Queue y Head Doorbell |

## 5.2.2 Controller Registers

[Table 125] Controller Capabilities

| Bits | Type | Name | Default Value | Description |
|---|---|---|---|---|
| 63:56 | RO | - | 0h | Reserved |
| 55:52 | RO | MPSMAX | 0h | Memory Page Size Maximum (Maximum is 4KB) |
| 51:48 | RO | MPSMIN | 0h | Memory Page Size Minimum (Minimum is 4KB) |
| 47:45 | RO | - | 0h | Reserved |
| 44:37 | RO | CSS | 1h | Command Sets Supported<br>1h: NVM command set |
| 36 | RO | NSSRS | 1h | NVM Subsystem Reset Supported |
| 35:32 | RO | DSTRD | 0h | Doorbell Stride<br>0: Stride of 4 bytes |
| 31:24 | RO | TO | 28h (960/1920GB)<br>32h (3840GB) | Timeout(unit:500ms)<br>28h: 20 seconds, 32h: 25 seconds |
| 23:19 | RO | - | 0h | Reserved |
| 18:17 | RO | AMS | 1h | Arbitration Mechanism Supported<br>(Weighted Round Robin with Urgent supported) |
| 16 | RO | CQR | 1h | Contiguous Queues Required |
| 15:0 | RO | MQES | 3FFFh | Maximum Queue Entries Supported<br>(16384 entries supported) |

[Table 126] Version

| Bits | Type | Name | Default Value | Description |
|---|---|---|---|---|
| 31:16 | RO | MJR | 1h | Major Version Number |
| 15:0 | RO | MNR | 400h | Minor Version Number |

**NOTE:**
The PM9A3 supports NVM Express version 1.4.

[Table 127] Interrupt Mask Set

| Bits | Type | Name | Default Value | Description |
|---|---|---|---|---|
| 31:0 | RW1S | IVMS | 0h | Interrupt Vector Mask Set |

[Table 128] Interrupt Mask Clear

| Bits | Type | Name | Default Value | Description |
|---|---|---|---|---|
| 31:00 | RW1C | IVMC | 0h | Interrupt Vector Mask Clear |

[Table 129] Controller Configuration

| Bits | Type | Name | Default Value | Description |
|---|---|---|---|---|
| 31:24 | RO | - | 0h | Reserved |
| 23:20 | RW | IOCQES | 0h | I/O Completion Queue Entry Size<br>(Configured as a power of 2)<br>(Should be set to 4 for a 16 byte entry size) |
| 19:16 | RW | IOSQES | 0h | I/O Submission Queue Entry Size<br>(Configured as a power of 2)<br>(Should be set to 6 for a 64 byte entry size) |
| 15:14 | RW | SHN | 0h | Shutdown Notification<br>0h: No notification<br>1h: Normal shutdown notification<br>2h: Abrupt shutdown notification<br>3h: Reserved<br>CSTS.SHST indicates shutdown status. |
| 13:11 | RW | AMS | 0h | Arbitration Mechanism Selected<br>0h: Round Robin<br>No other values supported. |
| 10:7 | RW | MPS | 0h | Memory Page Size<br>MPS is 2^(12+MPS)<br>Shall be within CAP.MPSMAX and CAP.MPSMIN ranges. |
| 6:4 | RW | CSS | 0h | Command Set Selected<br>0h: NVM Command Set<br>No other values supported |
| 3:1 | RO | - | 0h | Reserved |
| 0 | RW | EN | 0h | Enable<br>When set to 1, controller shall process commands.<br>When cleared to 0, controller shall not process commands.<br>This field is subject to CSTS.RDY and CAP.TO restrictions. |

[Table 130] Controller Status

| Bits | Type | Name | Default Value | Description |
|---|---|---|---|---|
| 31:6 | RO | - | 0h | Reserved |
| 5 | RW | PP | 0h | Processing Paused |
| 4 | RW1C | NSSRO | 0h | NVM Subsystem Reset Occurred |
| 3:2 | RO | SHST | 0h | Shutdown Status<br>0h: Normal operation, no shutdown requested<br>1h: Shutdown processing occurring<br>2h: Shutdown processing complete<br>3h: Reserved |
| 1 | RO | CFS | 0h | Controller Fatal Status |
| 0 | RO | RDY | 0h | 1h: Controller ready to process commands<br>0h: Controller shall not process commands. |

[Table 131] NVM Subsystem Reset

| Bits | Type | Name | Default Value | Description |
|---|---|---|---|---|
| 31:0 | RW | NSSRC- | 0h | NVM Subsystem Reset Control |

[Table 132] Admin Queue Attributes

| Bits | Type | Name | Default Value | Description |
|---|---|---|---|---|
| 31:28 | RO | - | 0h | Reserved |
| 27:16 | RW | ACQS | 0h | Admin Completion Queue Size<br>Max: 4096 (Value of 4095h - 0's based value) |
| 15:12 | RO | - | 0h | Reserved |
| 11:0 | RW | ASQS | 0h | Admin Submission Queue Size<br>Max: 4096 (Value of 4095h - 0's based value) |

[Table 133] Admin Submission Queue Base Address

| Bits | Type | Name | Default Value | Description |
|---|---|---|---|---|
| 63:12 | RW | ASQB | 0h | Admin Submission Queue Base Address |
| 11:0 | RO | - | 0h | Reserved |

[Table 134] Admin Completion Queue Base Address

| Bits | Type | Name | Default Value | Description |
|---|---|---|---|---|
| 63:12 | RW | ACQB | 0h | Admin Completion Queue Base Address |
| 11:0 | RO | - | 0h | Reserved |

[Table 135] Submission Queue Tail y Doorbell

| Bits | Type | Name | Default Value | Description |
|---|---|---|---|---|
| 31:16 | RO | - | 0h | Reserved |
| 15:0 | RW | SQT | 0h | Submission Queue Tail |

[Table 136] Completion Queue Head y Doorbell

| Bits | Type | Name | Default Value | Description |
|---|---|---|---|---|
| 31:16 | RO | - | 0h | Reserved |
| 15:0 | RW | CQH | 0h | Completion Queue Head |

# 6.0 SUPPORTED COMMAND SET

The Admin command sets and NVM I/O command sets of Samsung SSD PM9A3 are defined in compliant with NVM Express specification revision 1.4

## 6.1 Admin Command Set

The Admin command set is the commands that are submitted to the Admin Submission Queues. The detailed specifications are described in NVM Express specification document.

[Table 137] Opcode for Admin Commands

| Opcode (Hex) | Command Name |
|---|---|
| 00h | Delete I/O Submission Queue |
| 01h | Create I/O Submission Queue |
| 02h | Get Log Page |
| 04h | Delete I/O Completion Queue |
| 05h | Create I/O Completion Queue |
| 06h | Identify |
| 08h | Abort |
| 09h | Set Feature |
| 0Ah | Get Feature |
| 0Ch | Asynchronous Event Request |
| 0Dh | Namespace Management |
| 10h | Firmware Commit |
| 11h | Firmware Image Download |
| 14h | Device Self-test |
| 15h | Namespace Attachment |
| 18h | Keep Alive (Not support) |
| 19h | Directive Send |
| 1Ah | Directive Receive |
| 1Ch | Virtualization Management (Not support) |
| 1Dh | NVMe-MI Send (Not support) |
| 1Eh | NVMe-MI Receive (Not support) |
| 7Ch | Doorbell Buffer Config (Not support) |
| 80h - BFh | I/O Command Set Specific - B6h Get LBA Status (not support) |
| C0h - FFh | Vendor Specific |

## 6.1.1 Identify Command

The Identify Command returns the data described below.

[Table 138] Identify Controller Data Structure

| Bytes | O/M | Default Value | Description |
|---|---|---|---|
| 1:0 | M | 144Dh | PCI Vendor ID |
| 3:2 | M | 144Dh | PCI Subsystem Vendor ID |
| 23:4 | M | S############## | Serial Number(ASCII), # :Variables |
| 63:24 | M | SAMSUNG MZ1L2960HCJR-00A07 (960GB)<br>SAMSUNG MZ1L21T9HCLS-00A07 (1920GB)<br>SAMSUNG MZ1L23T8HBLA-00A07(3840GB) | Model Number (ASCII) |
| 71:64 | M | CS: NQxx<br>MP : NAxx | Firmware Revision, #:Variables |
| 72 | M | 2h | Recommended Arbitration Burst |
| 75:73 | M | 002538h | IEEE OUI |
| 76 | O | 0h | Multi-Interface Capabilties and Namespace Sharing Capability<br>Bit 2: 1h - Controller is associated with an SR-IOV Virtual Function<br>0h - Controller is associated with a PCI Function.<br>Bit 1: 1h - Device has Two or More controller<br>0h - Device has One Controller<br>Bit 0: 1h - Device has Two or More physical PCI Express ports<br>0h - Device has One PCI Express port |
| 77 | M | 9h | Maximum Data Transfer Size<br>9h: 2MB |
| 79:78 | M | 06h | Controller ID (CNTLID) |
| 83:80 | M | 0x10400 | Controller Version |
| 87:84 | M | 0x7A1200 | RTD3 Resume Laterncy |
| 91:88 | M | 0x7A1200 | RTD3 Entry Latancy |
| 95:92 | M | 300h | Optional Asynchronous Events Supported (OAES) |
| 99:96 | M | 80h | Controller Attributes (CTRATT)<br>Bit 7 (Namespace Granularity): Reporting of Namespace Granulari |
| 101:100 | O | 0h | Read Recovery Levels Supported (RRLS) |
| 110:102 | - | 0h | Reserved |
| 111 | M | 0h | Controller Type (CNTRLTYPE) |
| 127:112 | O | | FRU Globally Unique Identifier (FGUID) |
| 239:128 | | 0h | Reserved |
| 252:240 | M | - | NVMe Management Interface Specification for Definition |
| 253 | M | 1h | NVM Subsystem Report (NVMSR) |
| 254 | M | 0h | VPD Write Cycle Information (VWCI) |
| 255 | M | 1h | Management Endpoint Capabilities (MEC) |

| | | | |
|---|---|---|---|
| 257:256 | M | 5Fh | Optional Admin Command Support<br>Bits 15:10 are reserved.<br>Bit 9 if set to '1', then the controller supports the Get LBA Status capability (refer to section 8.22). If cleared to '0', then the controller does not support the Get LBA Status capability.<br>Bit 8 if set to '1', then the controller supports the Doorbell Buffer Config command. If cleared to '0', then the controller does not support the Doorbell Buffer Config command.<br>Bit 7 if set to '1', then the controller supports the Virtualization Management command. If cleared to '0', then the controller does not support the Virtualization Management command.<br>Bit 6 if set to '1', then the controller supports the NVMe-MI Send and NVMe-MI Receive commands. If cleared to '0', then the controller does not support the NVMe-MI Send and NVMe-MI Receive commands.<br>Bit 5 if set to '1' then the controller supports Directives. If cleared to '0' then the controller does not support Directives. A controller that supports Directives shall support the Directive Send and Directive Receive commands. Refer to section 9.<br>Bit 4 if set to '1' then the controller supports the Device Self-test command. If cleared to '0' then the controller does not support the Device Self-test command.<br>Bit 3: 1h - Namespace Management and Namespace Attachment Commands Supported<br>Bit 2: 1h – Firmware Activate/Download Supported<br>Bit 1: 1h Format NVM Supported<br>Bit 0: 1h Security Send and Security Receive Supported |
| 258 | M | 7h | Abort Command Limit<br>(Maximum number of concurrently outstanding Abort commands)<br>(0's based value) |
| 259 | M | 3h | Asynchronous Event Request Limit<br>(Maximum number of concurrently outstanding Asynchronous Event Request commands)<br>(0's based value) |
| 260 | M | 17h | Firmware Updates<br>Bits7:5–Reserved<br>Bits4– 1h Controller supports firmware activation without a reset 0h Controller requires a reset for firmware to be activated Bits3:1–Number of firmware slots<br>Bit 0 – 1h Slot 1 is read only |
| 261 | M | Eh | Log Page Attributes<br>Bits 7:5 are reserved.<br>Bit 4: Persistent Event log.<br>Bit 3: the Telemetry Host-Initiated and Telemetry Controller-Initiated log pages and sending Telemetry Log Notices.<br>Bit 2: extended data for the Get Log Page command.<br>Bit 1: the Commands Supported and Effects log page.<br>Bit 0: 0h SMART data is global for all namespaces |
| 262 | M | 3Fh | Error Log Page Entries<br>(Maximum number of Error Information log entries stored by controller)<br>(0's based value) |
| 263 | M | 0h | Number of Power States Support<br>(0's based value) |
| 264 | M | 1h | Admin Vendor Specific Command Configuration<br>Bits 7:1 – reserved<br>Bit 0 – Indicates Admin Vendor Specific Commands use the format defined in Admin and NVM Vendor Specific Commands (Optional) table of NVM Express spec. |
| 265 | O | 0h | Autonomous Power State Transition Attributes (APSTA) |
| 267:266 | M | 15Eh | Warning Composite Temperature Threshold |
| 269:268 | M | 166h | Critical Composite Temperature Threshold |
| 271:270 | O | 0h | Maximum Time for Firmware Activation |
| 275:272 | O | 0h | Host Memory Buffer Preferred Size |
| 279:276 | O | 0h | Host Memory Buffer Minimum Size |

| | | | |
|---|---|---|---|
| 295:280 | O | DF90356000h (960GB)<br>1BF1FC56000h (1920GB)<br>37E3EE56000h (3840GB) | Total NVM Capacity |
| 311:296 | O | 0h | Unallocated NVM Capacity |
| 315:312 | O | 0h | Replay Protected Memory Block Support(RPMBS) |
| 317:316 | O | 23h | Extended Device Self-test Time (EDSTT) |
| 318 | O | 1h | Device Self-test Options (DSTO) |
| 319 | M | 0h | Firmware Update Granularity (FWUG) |
| 321:320 | M | 0h | Keep Alive Support (KAS) |
| 323:322 | O | 0h | Host Controlled Thermal Management Attributes (HCTMA) |
| 325:324 | O | 0h | Minimum Thermal Management Temperature (MNTMT) |
| 327:326 | O | 0h | Maximum Thermal Management Temperature (MXTMT) |
| 331:328 | O | 3h | Sanitize Capabilities (SANICAP) |
| 335:332 | O | 0h | Host Memory Buffer Minimum Descriptor Entry Size (HMMINDS) |
| 337:336 | O | 0h | Host Memory Maximum Descriptors Entries (HMMAXD) |
| 339:338 | O | 0h | NVM Set Identifier Maximum (NSETIDMAX)<br>Non - IOD:0h, IOD:4h |
| 341:340 | O | 0h | Endurance Group Identifier Maximum (ENDGIDMAX) |
| 342 | O | 0h | ANA Transition Time (ANATT) |
| 343 | O | 0h | Asymmetric Namespace Access Capabilities (ANACAP) |
| 347:344 | O | 0h | ANA Group Identifier Maximum (ANAGRPMAX) |
| 351:348 | O | 0h | Number of ANA Group Identifiers (NANAGRPID) |
| 355:352 | O | 0h | Persistent Event Log Size (PELS) |
| 511:356 | - | - | Reserved |
| 512 | M | 66h | Submission Queue Entry Size<br>Bits 7:4 – 6h Max SQES (64 bytes)<br>Bits 3:0 – 6h Required SQES (64 bytes) |
| 513 | M | 44h | Completion Queue Entry Size<br>Bits 7:4 – 4h Max SQES (16 bytes)<br>Bits 3:0 – 4h Required SQES (16 bytes) |
| 515:514 | M | 100h | Maximum Outstanding Commands (MAXCMD) |
| 519:516 | M | 20h | Number of Namespaces |
| 521:520 | M | 5Fh | Optional NVM Command Support<br>Bits 15:8 - Reserved<br>Bit 7 - 1h Verify command Supported<br>0h Not support Verify command<br>Bit 6 - 1h Timestamp feature Supported<br>0h Not support the Timestamp feature<br>Bit 5 – 1h Reservations Supported<br>0h Not support Reservations<br>Bit 4 – 1h Save field in Set Feature & Select field in Get Feature Supported<br>0h Not support Save field in Set Feature & Select field in Get Feature<br>Bit 3 – 1h Write Zeros Supported<br>0h Not support Write Zeros<br>Bit 2 – 1h Dataset Management Supported<br>0h Not support Dataset Management<br>Bit 1 – 1h Write Uncorrectable Supported<br>0h Not support Write Uncorrectable<br>Bit 0 – 1h Compare Supported<br>0h Not support Compare |
| 523:522 | M | 0h | Fused Operation Support<br>Bits 15:1 – Reserved<br>Bit 0 – 0h Compare/Write Fused Operation Not Supported |
| 524 | M | 4h | Format NVM Attributes<br>Bits 7:3 – Reserved<br>Bit 2 – 1h Cryptographic Erase<br>Bit 1 – 1h Secure Erase Per Namespace<br>Bit 0 – 0h Format Per Namespace |

| | | | |
|---|---|---|---|
| 525 | M | 6h | Volatile Write Cache<br>0h – No VWC present |
| 527:526 | M | 3FFh | Atomic Write Unit Normal |
| 529:528 | M | 7h | Atomic Write Unit Power Fail (0's based value) |
| 530 | M | 1h | NVM Vendor Specific Command Configuration<br>Bits 7:1 – reserved<br>Bit 0 – Indicates NVM Vendor Specific Commands use the format defined in NVM Express specification |
| 531 | M | 0h | Reserved |
| 533:532 | O | 0h | ACWU |
| 535:534 | M | 0h | Reserved |
| 539:536 | O | 0h | No SGL support |
| 703:540 | - | 0h | Reserved |
| 767:704 | | 0h | Reserved |
| 1023:768 | | | NVM Subsystem NVMe Qualified Name (SUBNQN) |
| I/O Command Set Attributes | | | |
| 1791:1024 | - | 0h | Reserved |
| 2047:1792 | | | Refer to the NVMe over Fabrics specification |
| Power State Descriptors | | | |
| 2079:2048 | M | Refer to 'Identify Power State Descriptor Data Structure' | Power State 0 Descriptor |
| 3071:2080 | O | 0h | Power State 1 ~ 31 Descriptor (PSD1~N) |
| 3072 | O | 3h | Error Mode Capabilities (ERRCAP) |
| 3073 | - | 0h | Current Error Mode |
| 3075:3074 | O | 136h | Supports Debugging Feature on Error Mode |
| 3079:3076 | O | 0h | Reason for entering Error Mode. |
| 3087:3080 | O | LNUSRG39 | Option ROM Version |
| 3091:3088 | O | 2020/04/02 | Option ROM Build Date |
| 3092 | O | 1h | OEM Extended SMART Supported |
| 3278:3093 | | | Reserved |
| 3279 | M | 6h | Security Features Supported |
| Vendor Specific | | | |
| 4095:3280 | - | - | Samsung Reserved |

[Table 139] Identify Power State Descriptor Data Structure

| Bits | PS0 | Description |
|---|---|---|
| 255:184 | 0h | Reserved |
| 183:182 | 2h | Active Power Scale(APS) |
| 181:179 | 0h | Reserved |
| 178:176 | 2h | Active Power Workload(APW) |
| 175:160 | 339h | Active Power(ACTP) |
| 159:152 | 0h | Reserved |
| 151:150 | 2h | Idle Power Scale(IPS) |
| 149:144 | 0h | Reserverd |
| 143:128 | 12Ch | Idle Power(IDLP) |
| 127:125 | 0h | Reserved |
| 124:120 | 0h | Relative Write Latency |
| 119:117 | 0h | Reserved |
| 116:112 | 0h | Relative Write Throughput |
| 111:109 | 0h | Reserved |
| 108:104 | 0h | Relative Read Latency |
| 103:101 | 0h | Reserved |
| 100:96 | 0h | Relative Read Throughput |
| 95:64 | 46h | Exit Latency |
| 63:32 | 46h | Entry Latency |
| 31:26 | 0h | Reserved |
| 25 | 0h | Non-Operational State |
| 24 | 0h | Max Power Scale |
| 23:16 | 0h | Reserved |
| 15:00 | 339h | Maximum Power |

[Table 140] Identify Namespace Data Structure

| Bytes | O/M | Default Value | Description |
|---|---|---|---|
| 7:0 | M | 6FC81AB0h (960GB)<br>DF8FE2B0h (1920GB)<br>1BF1F72B0h (3840GB) | Namespace Size(512B) |
| 15:8 | M | 6FC81AB0h (960GB)<br>DF8FE2B0h (1920GB)<br>1BF1F72B0h (3840GB) | Namespace Capacity(512B) |
| 23:16 | M | 0h | Namespace Utilization<br>A device may report Namespace Utilization equal to Namespace Capacity at all times if the product is not targeted for thin provisioning environments |
| 24 | M | 12h | Namespace Features<br>Bits 7:5 are reserved.<br>Bit 4 if set to '1' indicates that the fields NPWG, NPWA, NPDG, NPDA, and NOWS are defined for this namespace and should be used by the host for I/O optimization; and NOWS defined for this namespace shall adhere to Optimal Write Size field setting defined in NVM Sets Attributes Entry for the NVM Set with which this namespace is associated. If cleared to '0', the controller does not support the fields NPWG, NPWA, NPDG, NPDA, and NOWS for this namespace; and Optimal Write Size field in NVM Sets Attributes Entry for the NVM Set with which this namespace is associated should be used by the host for I/O optimization.<br>Bit 3 if set to '1' indicates that the non-zero NGUID and non-zero EUI64 fields for this namespace are never reused by the controller. If cleared to '0', then the NGUID and EUI64 values may be reused by the controller for a new namespace created after this namespace is deleted. This bit shall be cleared to '0' if both NGUID and EUI64 fields are cleared to 0h. Refer to section 7.11.<br>Bit 2 if set to '1' indicates that the controller supports the Deallocated or Unwritten Logical Block error for this namespace. If cleared to '0', then the controller does not support the Deallocated or Unwritten Logical Block error for this namespace. Refer to section 6.7.1.1.<br>Bit 1 if set to '1' indicates that the fields NAWUN, NAWUPF, and NACWU are defined for this namespace and should be used by the host for this namespace instead of the AWUN, AWUPF, and ACWU fields in the Identify Controller data structure. If cleared to '0', then the controller does not support the fields NAWUN, NAWUPF, and NACWU for this namespace. In this case, the host should use the AWUN, AWUPF, and ACWU fields defined in the Identify Controller data structure in Figure 111. Refer to section 6.4.<br>Bit 0 if set to '1' indicates that the namespace supports thin provisioning. Specifically, the Namespace Capacity reported may be less than the Namespace Size. When this feature is supported and the Dataset Management command is supported, then deallocating LBAs shall be reflected in the Namespace Utilization field. Bit 0 if cleared to '0' indicates that thin provisioning is not supported and the Namespace Size and Namespace Capacity fields report the same value. |
| 25 | M | 1h | Number of LBA Formats |
| 26 | M | 0h | Formatted LBA Size<br>Bits 7:5 – Reserved<br>Bit 4 – Metadata interleaved or separate (based on LBA format)<br>Bit 3:0 – Indicates LBA format |
| 27 | M | 0h | Metadata Capabilities<br>Bits 7:2 – Reserved<br>Bit 1 – Supports Metadata as separate buffer<br>Bit 0 – Supports Metadata as extended LBA |
| 28 | M | 0h | End-to-end Data Protection Capabilities<br>Bits 7:5 – Reserved<br>Bit 4 – Supports protection information as last 8 bytes of Metadata<br>Bit 3 – Supports protection information as first 8 bytes of metadata<br>Bit 2 – Supports Type 3 protection information<br>Bit 1 – Supports Type 2 protection information<br>Bit 0 – Supports Type 1 protection information |
| 29 | M | 0h | End-to-End Data Protection Type Settings<br>Bits 7:4 – Reserved<br>Bit 3 – 1: Protection information transferred as first 8 bytes of metadata<br>Bit 3 – 0: Protection information transferred as last 8 bytes of metadata<br>Bit 2:0 – 000b: Protection information disabled<br>Bit 2:0 – 1h: Protection type 1 enabled<br>Bit 2:0 – 2h: Protection type 2 enabled<br>Bit 2:0 – 3h: Protection type 3 enabled |

| | | | |
|---|---|---|---|
| 30 | O | 0h | Namespace Multi-path I/O and Namespace sharing Capabilities (NMIC)<br>Bits 7:1 - Reserved<br>Bit 0 - 1 : Accessible by two or more controllers<br>Bit 0 - 0 : Private namespace |
| 31 | O | 0h | Reservation Capabilities (RESCAP)<br>Bits 7 - Reserved<br>Bits 6 - 1: Namespace supports the Exclusive Access (All Registrants reservation type)<br>Bit 5 - 1 : Namespace supports the Write Exclusive (All Registrants reservation type)<br>Bit 4 - 1 : Namespace supports the Exclusive Access (Registrants only reservation type)<br>Bit 3 - 1 : Namespace supports the Write Exclusive (Registrants only reservation type)<br>Bit 2 - 1 : Namespace supports the Exclusive Access Reservation type<br>Bit 1 - 1 : Namespace supports the Write Exclusive Reservation type<br>Bit 0 - 1 : Namespace supports the Persist Through Power Loss capability |
| 32 | O | 80h | Format Progress Indicator(FPI) |
| 33 | O | 9h | Deallocate Logical Block Features (DLFEAT) |
| 35:34 | O | 3FFh | Namespace Atomic Write Unit Normal |
| 37:36 | O | 7h | Namespace Atomic Write Unit Power Fail |
| 39:38 | O | 0h | Namespace Atomic Compare & Write Unit |
| 41:40 | O | 3FFh | Namespace Atomic Boundary Size Normal |
| 43:42 | O | 0h | Namespace Atomic Boundary Offset |
| 45:44 | O | 7h | Namespace Atomic Boundary Size Power Fail |
| 47:46 | O | 0h | Namespace Optimal I/O Boundary (NOIOB) |
| 63:48 | O | DF90356000h (960GB)<br>1BF1FC56000h (1920GB)<br>37E3EE56000h (3840B) | NVM Capacity (NVMCAP) |
| 65:64 | O | FFh | Namespace Preferred Write Granularity (NPWG) |
| 67:66 | O | 7h | Namespace Preferred Write Alignment (NPWA) |
| 69:68 | O | FFh | Namespace Preferred Deallocate Granularity (NPDG) |
| 71:70 | O | 7h | Namespace Preferred Deallocate Alignment (NPDA) |
| 73:72 | O | FFh | Namespace Optimal Write Size (NOWS) |
| 99:74 | O | 0h | Reserved |
| 101:100 | O | 0h | NVM Set Identifier (NVMSETID) |
| 103:102 | O | 0h | Endurance Group Identifier (ENDGID) |
| 119:104 | O | Update by Vendor Command | Namespace Globally Unique Identifier (NGUID)<br>#:Variables<br>*NGUID specifies data in a big endian format. |
| 127:120 | O | 0h | IEEE Extended Unique Identifier(EUI64)<br>#:Variables<br>*EUI64 specifies data in a big endian format. |
| 131:128 | M | Refer to 'LBA Format 0 Data Structure' | LBA Format 0 Support |
| 135:132 | O | Refer to 'LBA Format 1 Data Structure' | LBA Format 1 Support |
| 139:136 | O | 0h | LBA Format 2 Support |
| 143:140 | O | 0h | LBA Format 3 Support |
| 147:144 | O | 0h | LBA Format 4 Support (N/A) |
| … | | | |
| 191:188 | O | 0h | LBA Format 15 Support (N/A) |
| 383:192 | - | 0h | Reserved |
| Vendor Specific | | | |
| 4095:384 | - | - | Samsung Reserved |

[Table 141] LBA Format 0 Data Structure

| Bits | Name | Default Value | Description |
|---|---|---|---|
| 31:26 | - | 0h | Reserved |
| 25:24 | RP | 0h | Relative Performance |
| 23:16 | LBADS | 9h | LBA Data Size |
| 15:00 | MS | 0h | Metadata Size |

[Table 142] LBA Format 1 Data Structure

| Bits | Name | Default Value | Description |
|---|---|---|---|
| 31:26 | - | 0h | Reserved |
| 25:24 | RP | 0h | Relative Performance |
| 23:16 | LBADS | Ch | LBA Data Size |
| 15:00 | MS | 0h | Meta data Size |

# 6.2 NVM Express I/O Command Set

[Table 143] Opcode for NVM Express I/O Commands

| Opcode (Hex) | Command Name |
|---|---|
| 00h | Flush |
| 01h | Write |
| 02h | Read |
| 04h | Write Uncorrectable |
| 05h | Compare |
| 08h | Write Zeroes |
| 09h | Dataset Management |

**NOTE:**
1) Deallocate feature in Dataset Management command is only supported in the Samsung SSD PM9A3.

# 6.3 SMART/Health Information

[Table 144] SMART/Health Information Log

| Bytes | Default Value | Attribute Description |
|---|---|---|
| 0 | 0 | Critical Warning<br>Bit 7:5 – Reserved<br>Bit 4 – 1h: the volatile memory backup device has failed.<br>(only valid if the controller has a volatile memory backup solution)<br>Bit 3 – 1h: the media has been placed in read only mode<br>Bit 2 – 1h: the device reliability has been degraded due to significant media related errors or any internal error that degrades device reliability<br>Bit 1 – 1h: the temperature has exceeded a critical threshold<br>Bit 0 – 1h: the available spare space has fallen below the threshold |
| 2:1 | Current Temp | Temperature |
| 3 | 100 | Available Spare |
| 4 | 10 | Available Spare Threshold |
| 5 | 0 | Percentage Used |
| 31:6 | - | Reserved |
| 47:32 | 0 | Data Units Read |
| 63:48 | 0 | Data Units Written |
| 79:64 | 0 | Host Read Commands |
| 95:80 | 0 | Host Write Commands |
| 111:96 | 0 | Controller Busy Time |
| 127:112 | 0 | Power Cycles |
| 143:128 | 0 | Power On Hours |
| 159:144 | 0 | Unsafe Shutdowns |
| 175:160 | 0 | Media Errors |
| 191:176 | 0 | Number of Error Information Log Entries |
| 195:192 | 0 | Warning Composite Temperature Time |
| 199:196 | 0 | Critical Composite Temperature Time |
| 201:200 | Current Temp | Temperature Sensor 1 |
| 203:202 | Current Temp | Temperature Sensor 2 |
| 205:204 | - | Temperature Sensor 3 |
| 207:206 | - | Temperature Sensor 4 |
| 209:208 | - | Temperature Sensor 5 |
| 211:210 | - | Temperature Sensor 6 |
| 213:212 | - | Temperature Sensor 7 |
| 215:213 | - | Temperature Sensor 8 |
| 511:216 | - | Reserved |

# 6.4 Extended SMART Information

[Table 145] Extended SMART Information Log (LID : 0xCA)

| Bytes | Default Value | Attribute Description |
|---|---|---|
| 2:0 | ABh | Lifetime Program Fail Cnt ID |
| 4:3 | 64h | Lifetime Program Fail Cnt Normalized Value |
| 11:5 | 0h | Lifetime Program Fail Cnt Current Raw Value |
| 14:12 | ACh | Lifetime Erase Fail Cnt ID |
| 16:15 | 64h | Lifetime Erase Fail Cnt Normalized Value |
| 23:17 | 0h | Lifetime Erase Fail Cnt Current Raw value |
| 26:24 | ADh | Lifetime Wearlevel Cnt ID |
| 28:27 | 64h | Lifetime Wearlevel Cnt Normalized Value |
| 35:29 | 0h | Lifetime Wearlevel Cnt Current Raw value<br>Bytes 1-0: Min. erase cycles<br>Bytes 3-2: Max. erase cycles<br>Bytes 5-4: Avg. erase cycles |
| 38:36 | B8h | Lifetime E2E Error Cnt ID |
| 40:39 | 64h | Lifetime E2E Error Cnt Normalized Value |
| 47:41 | 0h | Lifetime E2E Error Cnt Current Raw Value |
| 50:48 | C7h | Lifetime CRC Error Cnt ID |
| 52:51 | 64h | Lifetime CRC Error Cnt Normalized Value |
| 59:53 | 0h | Lifetime CRC Error Cnt Current Raw Value |
| 62:60 | E2h | Media Wear Percentage ID |
| 64:63 | 64h | Media Wear Percentag Normalized Value |
| 71:65 | 0h | Media Wear Percentag Current Raw Value |
| 74:72 | E3h | Host Read Percentage ID |
| 76:75 | 64h | Host Read Percentage Normalized Value |
| 83:77 | 0h | Host Read Percentage Current Raw Value |
| 86:84 | E4h | Workload Timer ID |
| 88:87 | 64h | Workload Timer Normalized Value |
| 95:89 | 0h | Workload Timer Current Raw Value |
| 98:96 | EAh | Lifetime Thermal Throttle Status ID |
| 100:99 | 64h | Lifetime Thermal Throttle Status Normalized Value |
| 107:101 | 64h | Lifetime Thermal Throttle Status Current Raw Value<br>Bytes 0: Throttle status reported as integer percentage.<br>Bytes 1-4: Throttling event count. Number of times thermal throttle has activated. Preserved over power cycles.<br>Byte 5: Reserved. |
| 131:108 | 0 | Reserved |
| 134:132 | F4h | Lifetime Physical Pages Written Cnt ID |
| 136:135 | 64h | Lifetime Physical Pages Written Cnt Normalized Value |
| 143:137 | 0h | Lifetime Physical Pages Written Cnt Current Raw Value |
| 146:144 | F5h | Lifetime Data Unit Written ID |
| 148:147 | 64h | Lifetime Data Unit Written Normalized Value |
| 155:149 | 0h | Lifetime Data Unit Written Current Raw Value |
| 255:156 | 0h | Reserved |
| 259:256 | 0h | Lifetime write amplification factor |
| 263:260 | 0h | Trailing hour write amplification factor |
| 279:264 | 0h | Lifetime user writes |
| 295:280 | 0h | Lifetime NAND writes |
| 311:296 | 0h | Lifetime user reads |
| 315:312 | 0h | Lifetime retired block count |

| | | |
|---|---|---|
| 317:316 | Current Temperature | Current temperature |
| 319:318 | Cap health | Capacitor health |
| 323:320 | Lifetime Unused Reserved Block | Lifetime Unused Reserved Block |
| 331:324 | 0h | Read Reclaim count |
| 339:332 | 0h | Lifetime UECC count |
| 343:340 | 0h | Lifetime Used Reserved Block |
| 359:344 | 0h | Power on hours |
| 375:360 | 0h | Lifetime clean shutdown count on power loss(NPO count) |
| 391:376 | 0h | Lifetime unclean shutdowns on power loss(SPO count) |
| 395:392 | 0h | Perf Indicator |
| 399:396 | 0h | WearLevel Count |
| 403:400 | 0h | HW Error Type |
| 407:404 | 0h | DeviceFail Recovery Count (Incomplete Shutdown) |
| 411:408 | 0h | SRAM CECC Count (CoreSRAM) |
| 415:412 | 0h | SRAM CECC Address (CoreSRAM) |
| 419:416 | 0h | SRAM CECC Count (Buffer) |
| 423:420 | 0h | SRAM CECC Address (Buffer) |
| 427:424 | 0h | DRAM CECC Count |
| 435:428 | 0h | DRAM CECC Address |
| 439:436 | 0h | DRAM UECC Count |
| 447:440 | 0h | DRAM UECC Address |
| 451:448 | 0h | E2E Error Count |
| 453:452 | 0h | FW Update Success Sount |
| 455:454 | 0h | FW Update Fail Count |
| 459:456 | Highest temperature | Highest Temperature |
| 463:460 | Lowest Temperature | Lowest Tempreature |
| 471:464 | 0h | Read Recovery Attempts |
| 479:472 | 0h | Reset Count |
| 495:480 | 0h | Trimmed Sector Count |
| 499:496 | 0h | Security Meta Erase Fail Count |
| 503:500 | 0h | Over Temperature Count |
| 507:504 | 0h | Under Temperature Count |
| 511:508 | 0h | Recovery Reset Count |

[Table 146] Enhanced SMART Log (LID : 0xC4)

| Bytes | Default Value | Attribute Description |
|---|---|---|
| 1:0 | 0h | Throughput Performance |
| 2 | 0h | Timed Workload Media Wear |
| 3 | 0h | Times Workload Host Read/Write Ratio |
| 5:4 | 0h | Read Error Rate |
| 7:6 | 0h | Write Error Rate |
| 11:8 | 0h | Unrecoverable Write Errors |
| 15:12 | 0h | Read Recovery Attempts |
| 17:16 | Temperature | Average Short Term Temperature |
| 19:18 | Temperature | Average Long Term Temperature |
| 21:20 | Temperature | Highest Temperature |
| 23:22 | Temperature | Lowest Temperature |
| 25:24 | Temperature | Highest Average Short Term Temperature |
| 27:26 | Temperature | Lowest Average Short Term Temperature |
| 29:28 | Temperature | Highest Average Long Term Temperature |
| 31:30 | Temperature | Lowest Average Long Term Temperature |
| 33:32 | 15Eh | Specified Maximum Operating Temperature |
| 35:34 | 111h | Specified Minimum Operating Temperature |
| 39:36 | 0h | Time in Over Temperature in Minutes |
| 55:40 | 0h | Physical Media Units Written |
| 71:56 | 0h | Physical Media Units Read |
| 77:72 | 0h | Bad User NAND block count (Raw) |
| 79:78 | 64h | Bad User NAND block count (Normalized) |
| 85:80 | 0h | Bad System NAND block count (Raw) |
| 87:86 | 64h | Bad System NAND block count (Normalized) |
| 91:88 | 0h | End to End Correction Counts (Detected Errors) |
| 95:92 | 0h | End to End Correction Counts (Corrected Errors) |
| 96:96 | 0h | System data % used |
| 97:97 | 64h | % Free Blocks |
| 105:98 | 0h | Unaligned I/O |
| 113:106 | 0h | Security Version Number |
| 121:114 | 0h | NUSE |
| 137:122 | 0h | PLP Start Count |
| 153:138 | Capacity specific | Endurance Estimate |
| 157:154 | 0h | BAD TLP Count |
| 161:158 | 0h | BAD DLLP Count |
| 165:162 | 0h | PHY Error Count |
| 169:166 | 0h | Thermal Protection Count |
| 173:170 | 0h | Thermal Shutdown Count |
| 511:174 | 0h | Reserved |

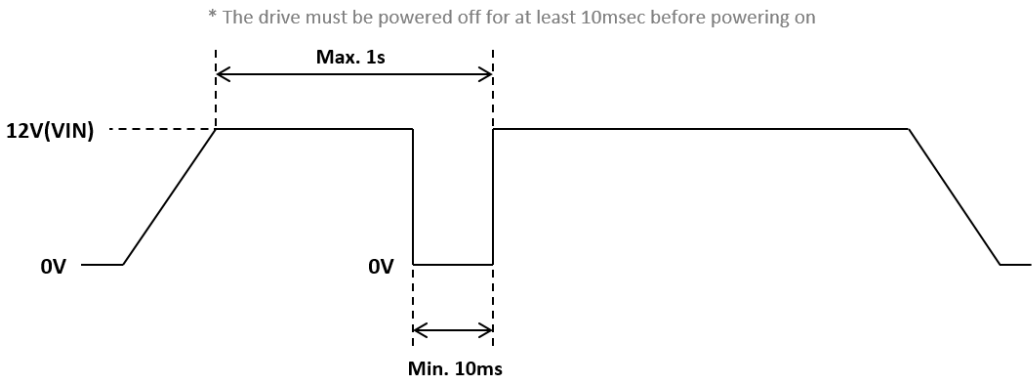
# 7.0 SPOR Specification (Sudden Power Off and Recovery)

## 7.1 Data Recovery in Sudden Power off

If power interruption is detected, SSD dumps all cached user data and meta data to NAND Flash. SSD could protect even the user data in DRAM from sudden power off while SSD is used with cache on. Commonly, data is protected all of the operation period.

## 7.2 Minimum Off time

In sudden power off case, minimum 10ms off time is required for stability




## 7.3 Time to Ready Sequence

In normal power-off recovery status, SSD needs less than 8 seconds to reach operating mode where SSD works perfectly with cache-on state. SSD is ready to respond identify Device command during FTL OPEN. When the sudden power-off occurs, the user data in DRAM will be dumped into the NAND Flash using the stored power in the capacitor. In sudden power-off recovery condition, mapping data will be loaded or the FTL meta data be rebuilt perfectly for initial max. 10 seconds. During this period, Identify Device command is still supported. It is called SPOR. (Sudden Power Off and Recovery)

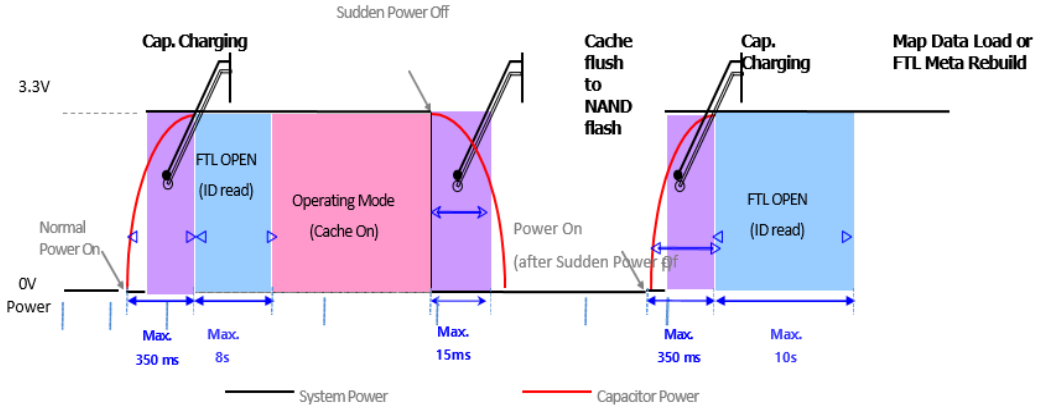



**Figure 3. Sudden Power on-off operation**

[Table 147] Device Ready Time for Normal Read / Write Operation after Sudden Power Off

| | 960GB | 1920GB | 3840GB |
|---|---|---|---|
| Open Time (sec) | 10s | 10s | 20s |

# 8.0 UEFI EXPANSION ROM

The expansion ROM integrated in Samsung SSD PM9A3 supports booting UEFI operating system

## 8.1 Supported Operating Systems

| Index | Operating Systems bootable on PM9A3 drive |
|---|---|
| 1 | RHEL 7.2 (Kernel 3.10.327) |
| 2 | RHEL 7.6 (Kernel 3.10.957) |
| 3 | CentOS 7.3 (Kernel 3.10.0-514) |
| 4 | CentOS 7.6 (Kernel 3.10.0-957) |
| 5 | Ubuntu 16.10 (Kernel 4.08) |
| 6 | Ubuntu 18.10 (Kernel 4.18) |
| 7 | Windows server 2016 |
| 8 | Windows server 2019 |

# 9.0 PRODUCT COMPLIANCE

## 9.1 Product regulatory compliance and Certifications

[Table 148] Certifications and Declarations

| Category | Certifications |
|---|---|
| Safety | c-UL-us |
| | CE |
| | TUV |
| | CB |
| EMC | CE (EU) |
| | BSMI (Taiwan) |
| | KC (South Korea) |
| | VCCI (Japan) |
| | RCM (Australia) |
| | FCC (USA) |
| | IC (CANADA) |

The three existing compliance marks (C-Tick, A-Tick and RCM) are consolidated into a single compliance mark - the RCM.

Caution: Any changes or modifications in construction of this device which are not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications, However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Modifications not expressly approved by the manufacturer could void the user's authority to operated the equipment under FCC rules.

1. 기자재 명칭 : SSD (Solid State Drive)
2. 모델명(Model): 라벨 별도 표기
3. 제조연월 : 라벨 별도 표기
4. 제조자 : 삼성전자(주)
5. 제조국가 : 대한민국
6. 상호명 : 삼성전자(주)

Industry Canada ICES-003 Compliance Label:
CAN ICES-3 (B)/NMB-3(B)

# 10.0 References

[Table 149] Standards References

| Item | Website |
|---|---|
| PCI Express Base Specification Revision 3.1 | http://www.pcisig.com/specifications/pciexpress/base3/ |
| PCI Express CEM Specification Revision 3.0 | http://www.pcisig.com/specifications/ |
| NVM Express Specification Rev. 1.4 | http://www.nvmexpress.org/ |
| NVM Express Management Interface, Revision 1.1a | http://www.nvmexpress.org/ |
| Enterprise SSD Form Factor Version 1.0a | http://www.ssdformfactor.org/ |
| Solid-State Drive Requirements and Endurance Test Method (JESD218A) | http://www.jedec.org/standards-documents/docs/jesd218a |
| Solid-State Drive Requirements and Endurance Test Method (JESD219A) | http://www.jedec.org/standards-documents/docs/jesd219a |